Analog Mixed Signal Circuits: From Neurons to Networks

Nima Maghari

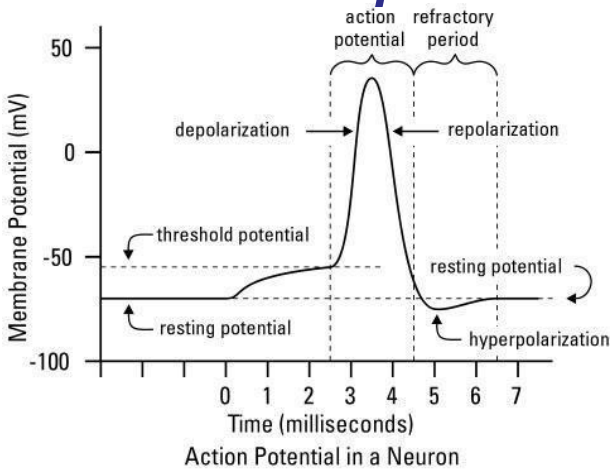
UF AMS LAB

University of Florida

Why Analog!

- **Signals in nature are in "Analog" form**

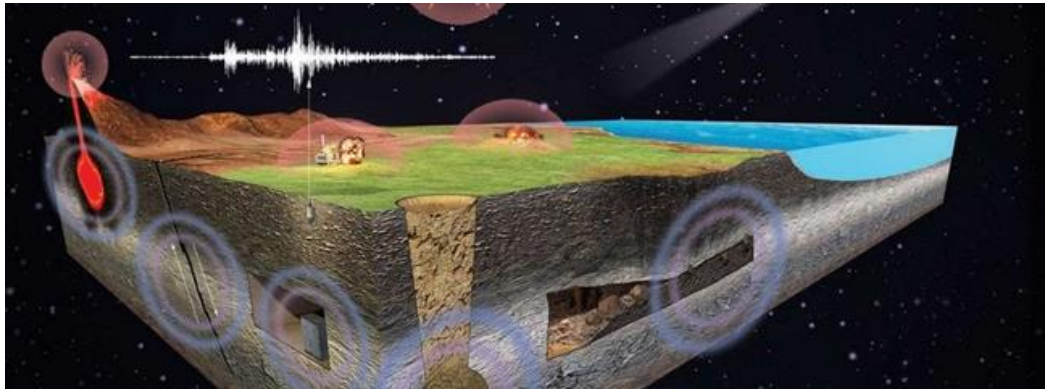
Neuron "spikes"



Action Potential in a Neuron

Audio

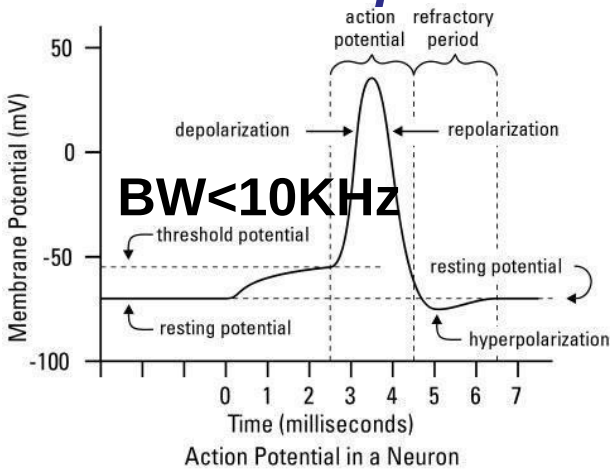
Seismic



Why Analog!

- **Signals in nature are in "Analog" form**

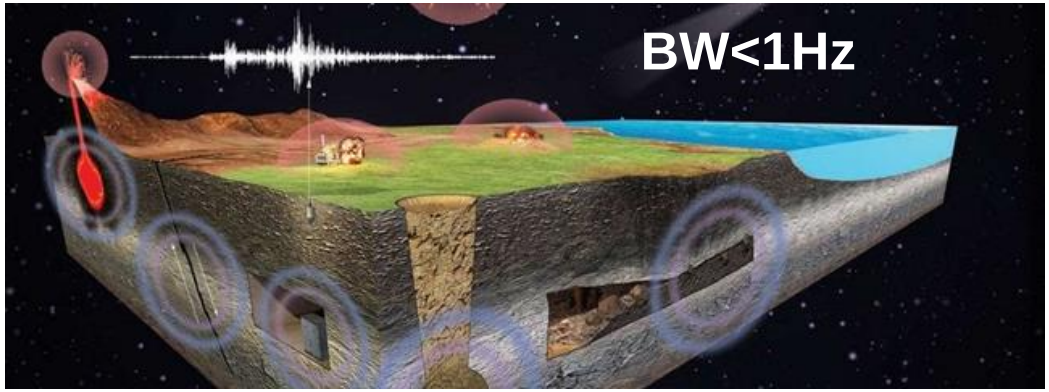
Neuron "spikes"



Action Potential in a Neuron

Audio

Seismic



Natural signals often tend to have low/very low BW

We Invented it!

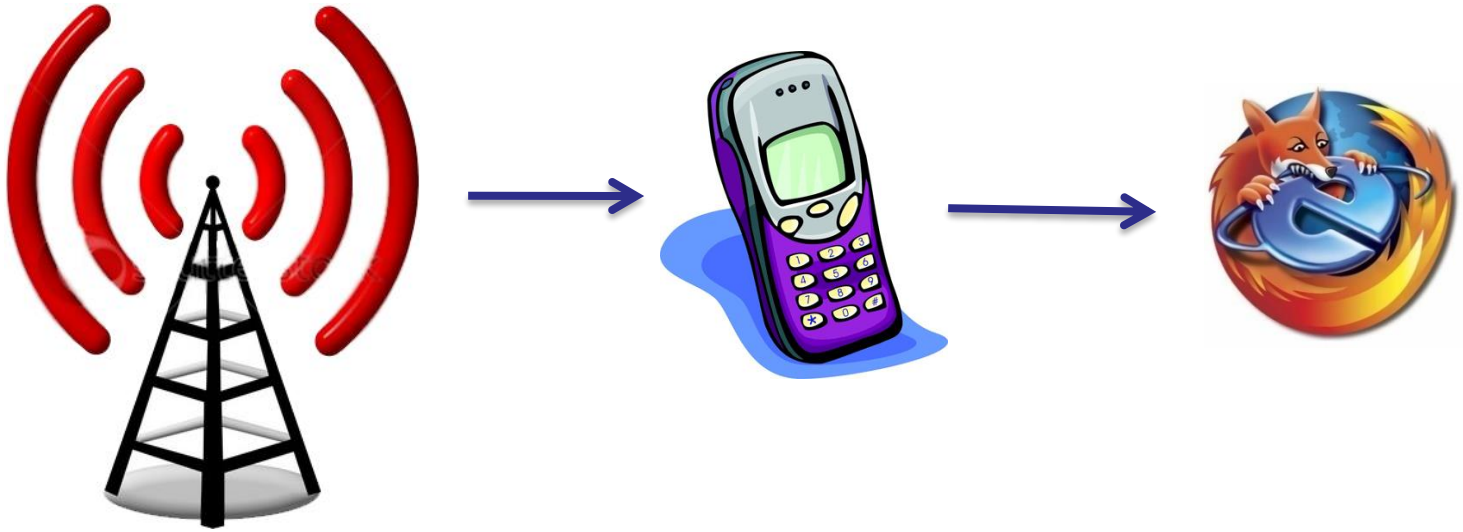
- **We are living in a “Digital” era where everything and anything can be digitized!**

We Invented it!

- **We are living in a "Digital" era where everything and anything can be digitized!**

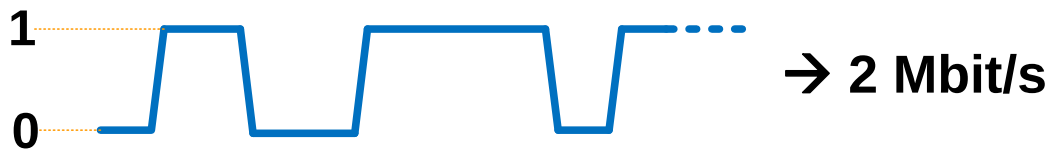
Digital Communication

- **Early generations**
  - **Analog modulations**
- **Modern generations**
  - **Digital modulation**
- **Everything is *Digital***



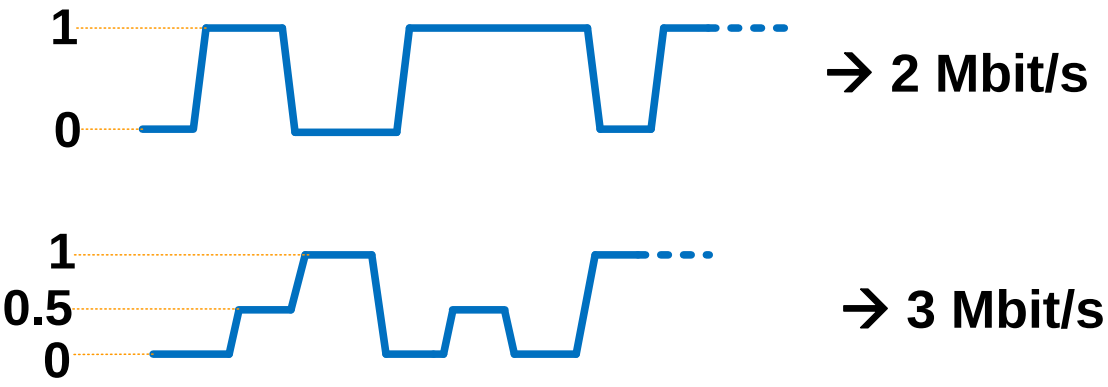
Transmission

- **Federal Communication Commission (FCC)**
  - **Assign bandwidth 1GHz**
    - **500 channels → 2 MHz/channel**



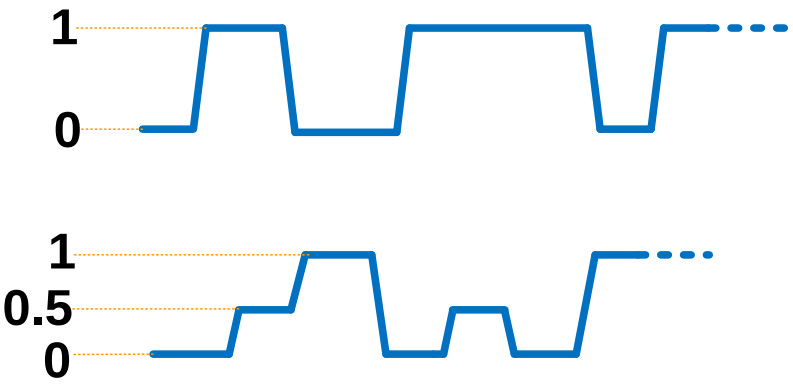
Transmission

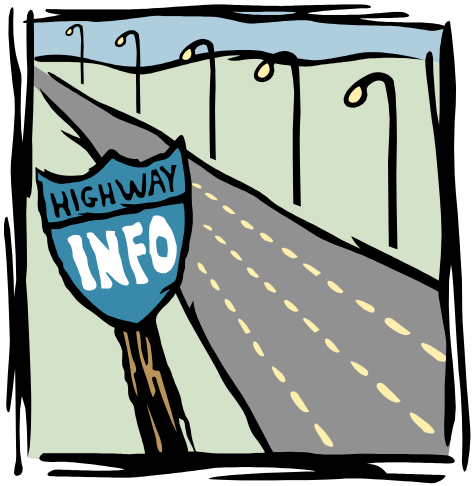
- **Federal Communication Commission (FCC)**
  - **Assign bandwidth 1GHz**
    - **500 channels → 2 MHz/channel**



Transmission

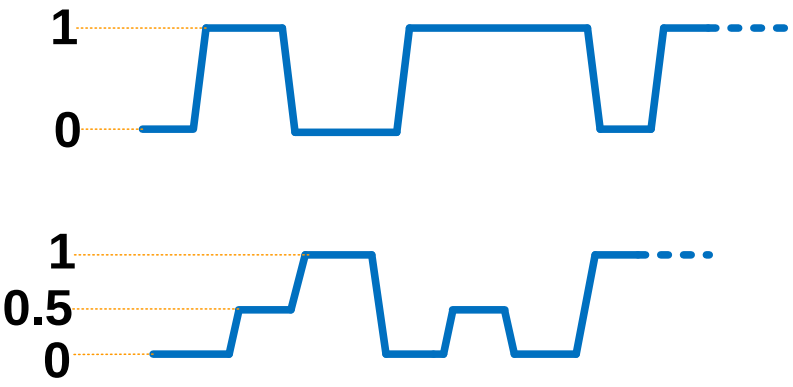
- **Federal Communication Commission (FCC)**
  - **Assign bandwidth 1GHz**
    - **500 channels → 2 MHz/channel**

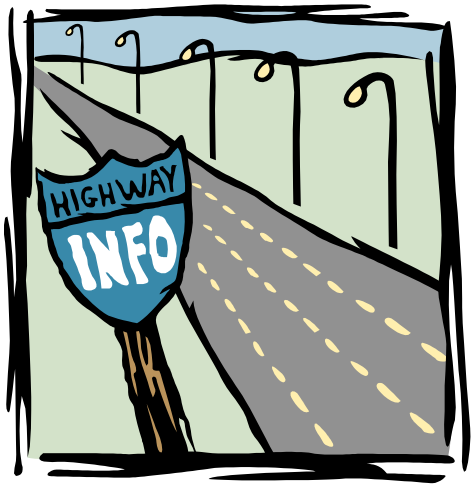




Transmission

- **Federal Communication Commission (FCC)**
  - **Assign bandwidth 1GHz**
    - **500 channels → 2 MHz/channel**

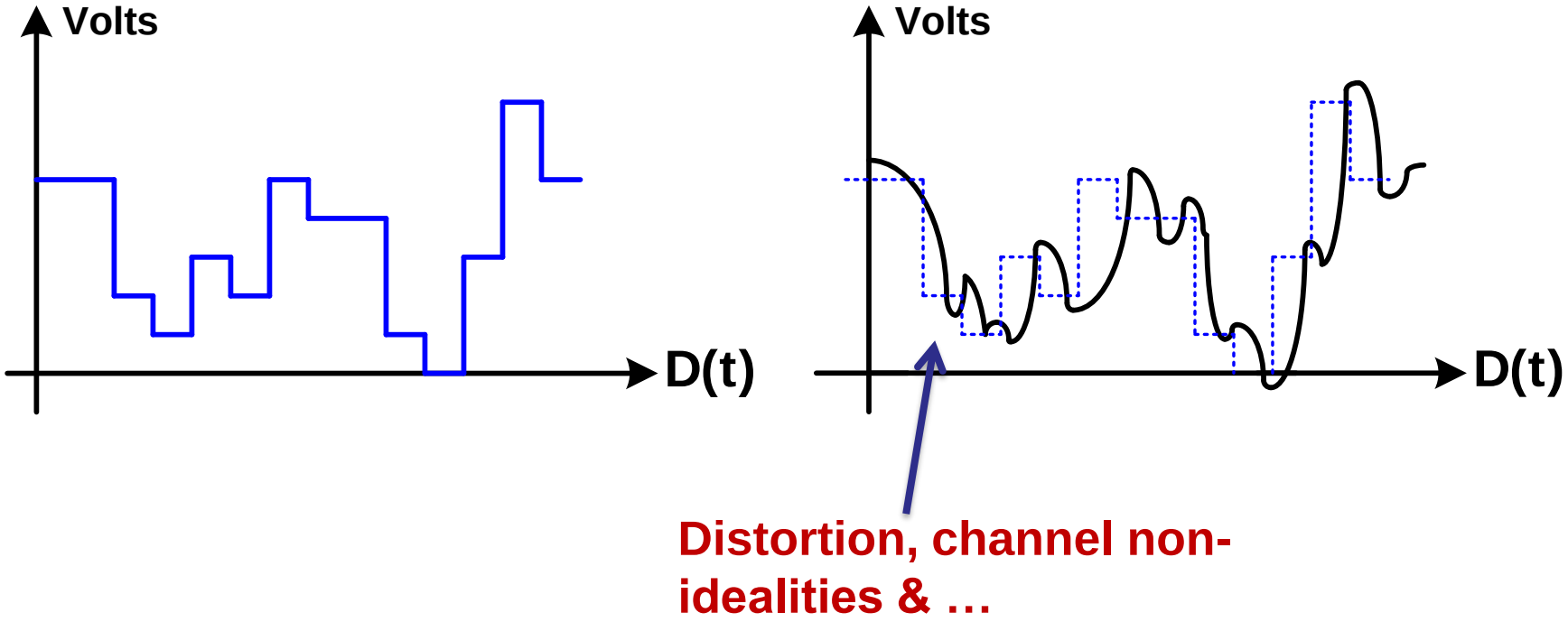




  - **Modern schemes transmit many more levels**

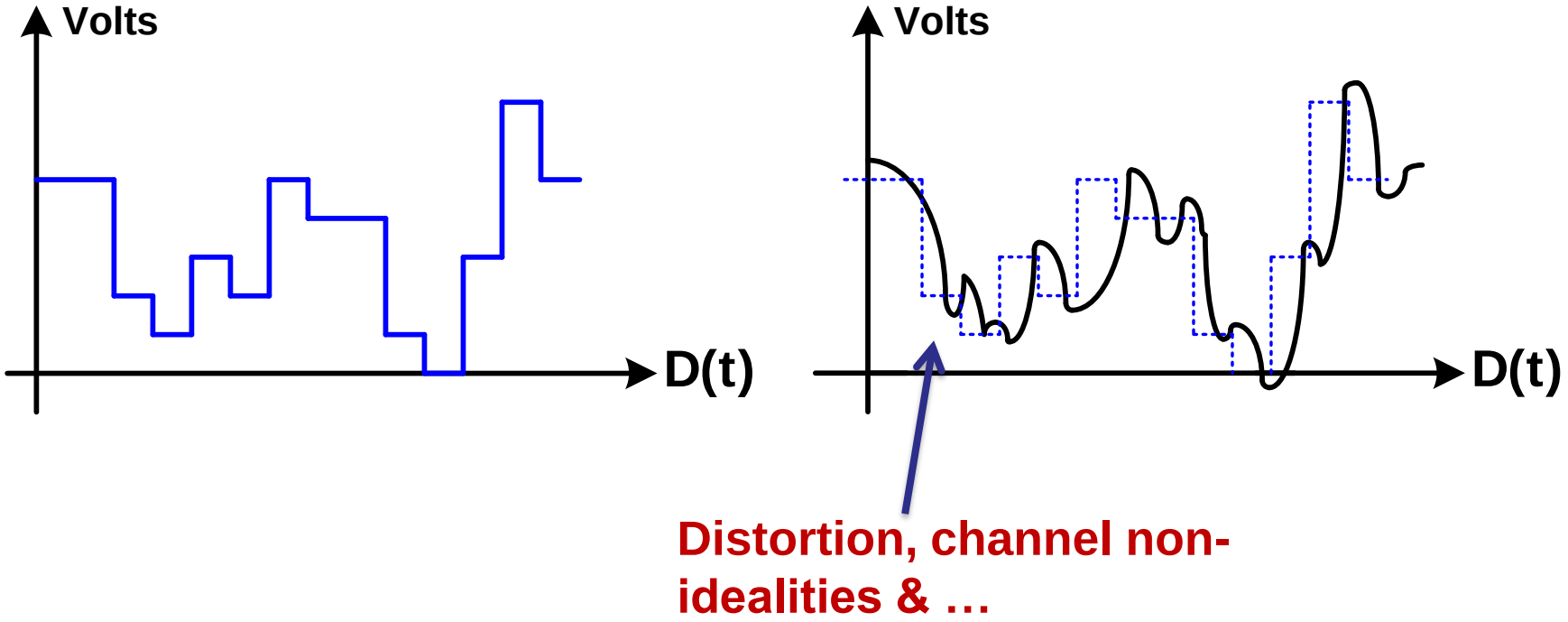
Transmission

- **8-level transmission**
  - **Ideally an 8-level ADC is sufficient to recover data**



Transmission

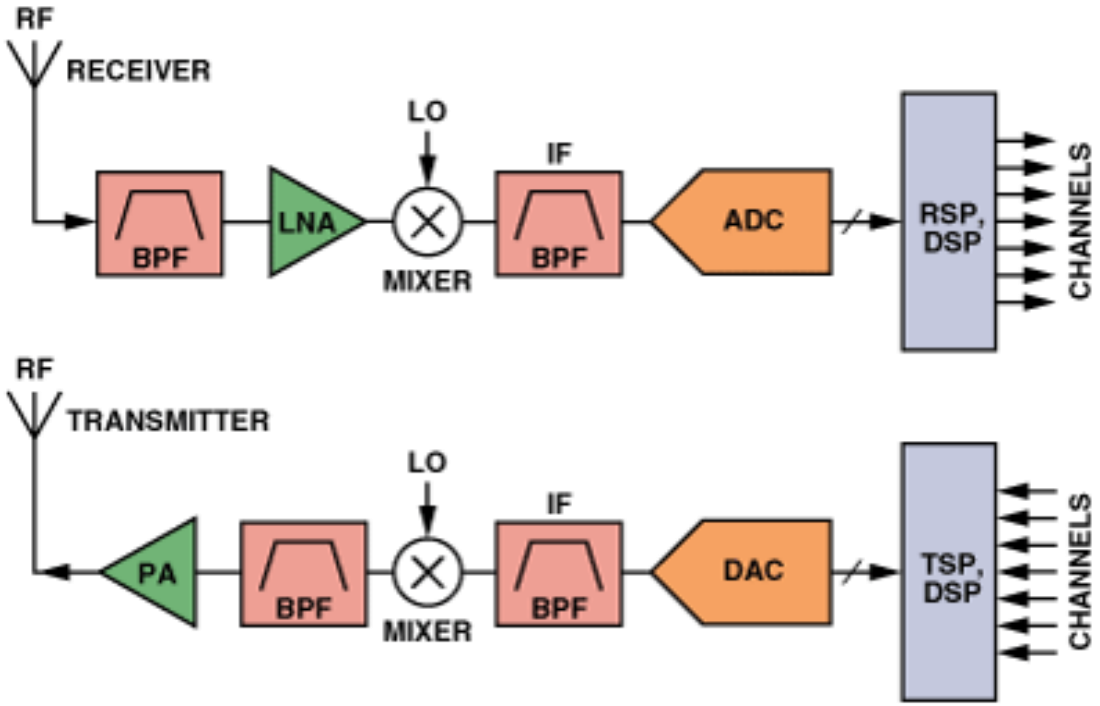
- **8-level transmission**
  - **Ideally an 8-level ADC is sufficient to recover data**



  - **The signal tends to look more analog than digital!**

Transmission

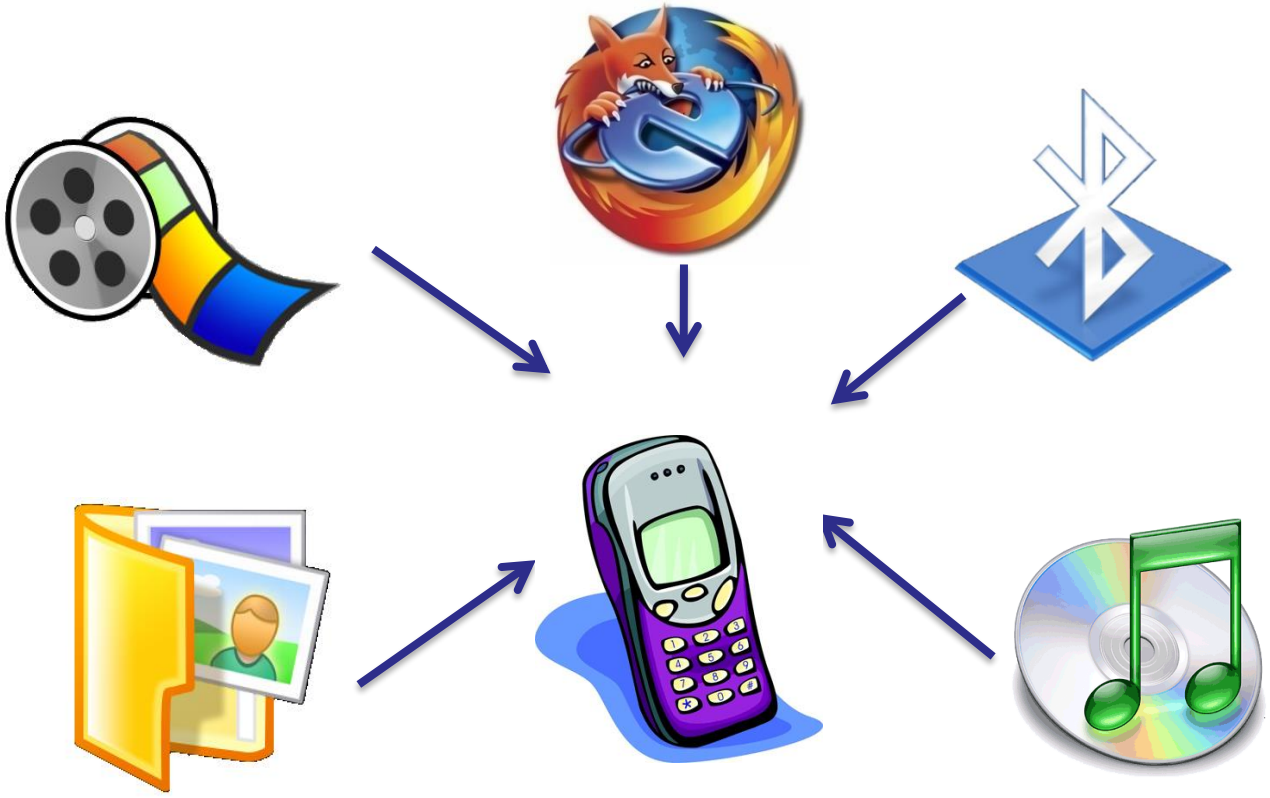
- **8-level transmission**
  - **Ideally an 8-level ADC is sufficient to recover data**



  - **The signal tends to look more analog than digital!**
  - **For both transmission and receiver we need Analog!**

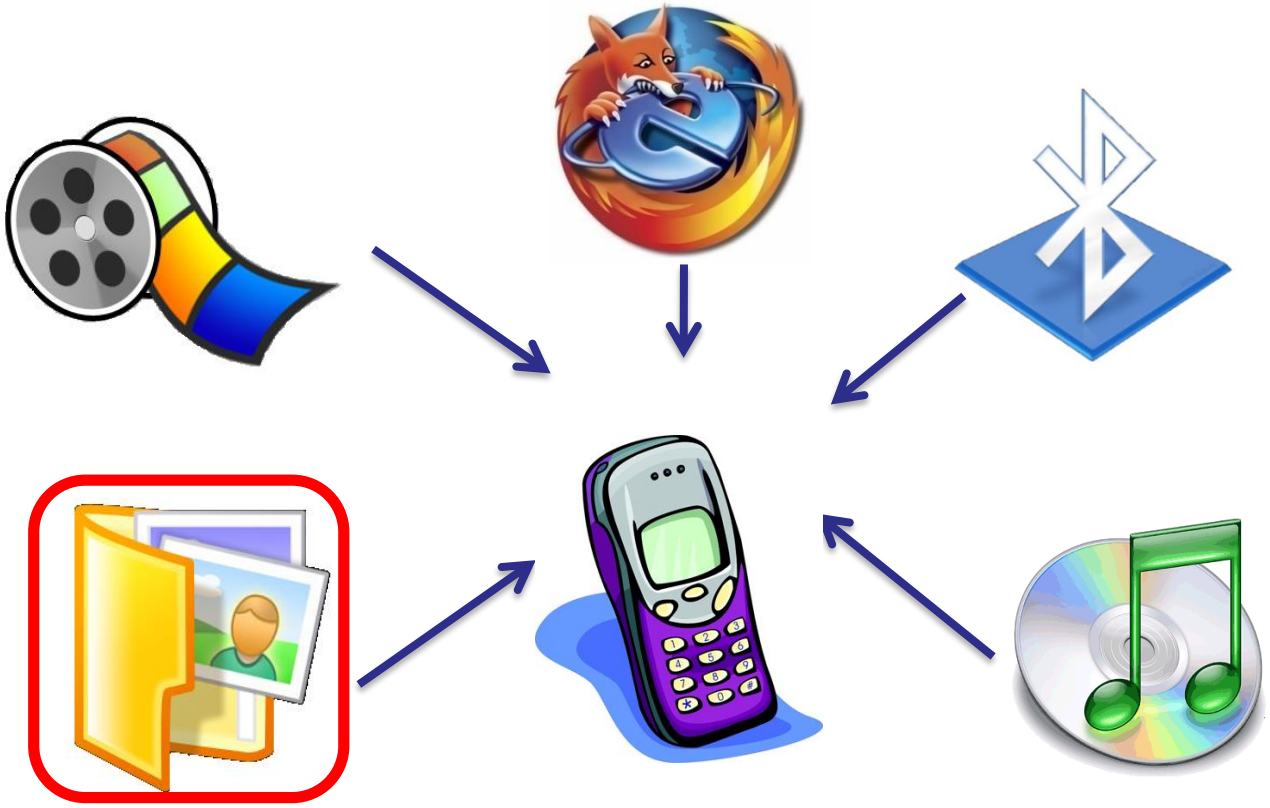
Background

- **Different applications. demand diff. specs**
  - **High bandwidth for data**
  - **High quality for audio**



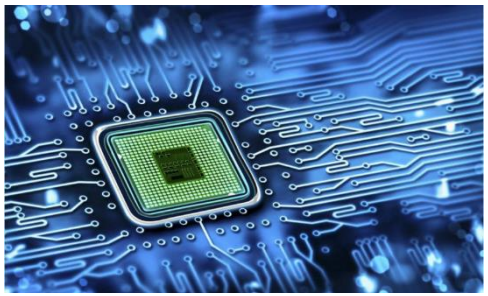
Background

- **Different applications. demand diff. specs**
  - **High bandwidth for data**
  - **High quality for audio**



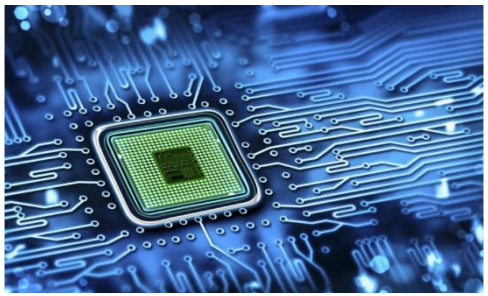
Digital Links

- **In ALL digital systems such as PC**
  - **All communication between ICs are digital**



Digital Links

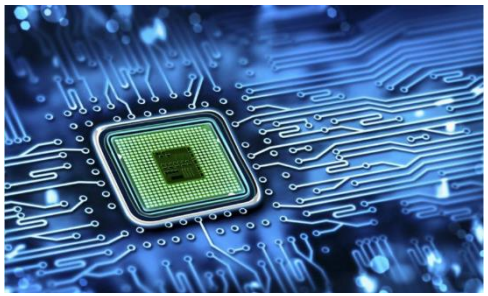
- **In ALL digital systems such as PC**
  - **All communication between ICs are digital**

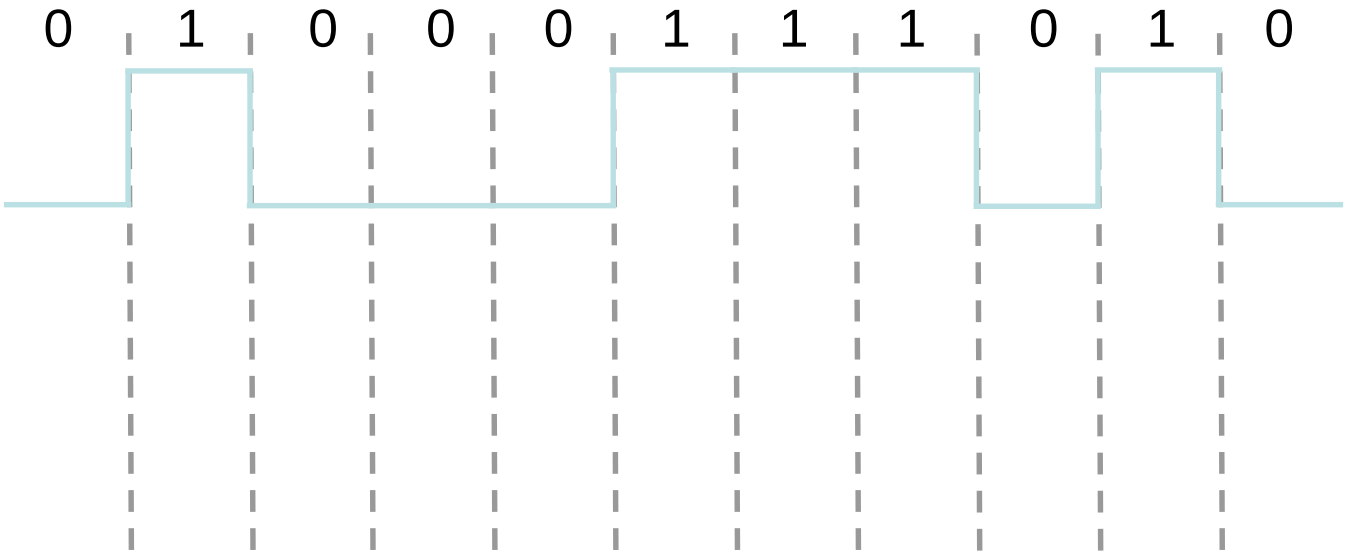


0 1 0 0 0 1 1 1 0 1 0

Digital Links

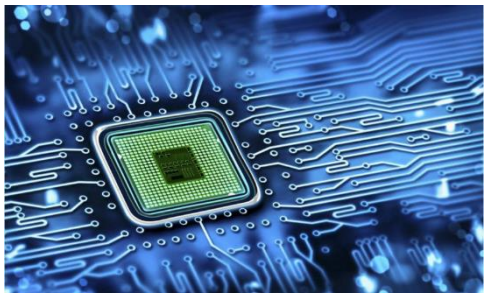
- **In ALL digital systems such as PC**
  - **All communication between ICs are digital**

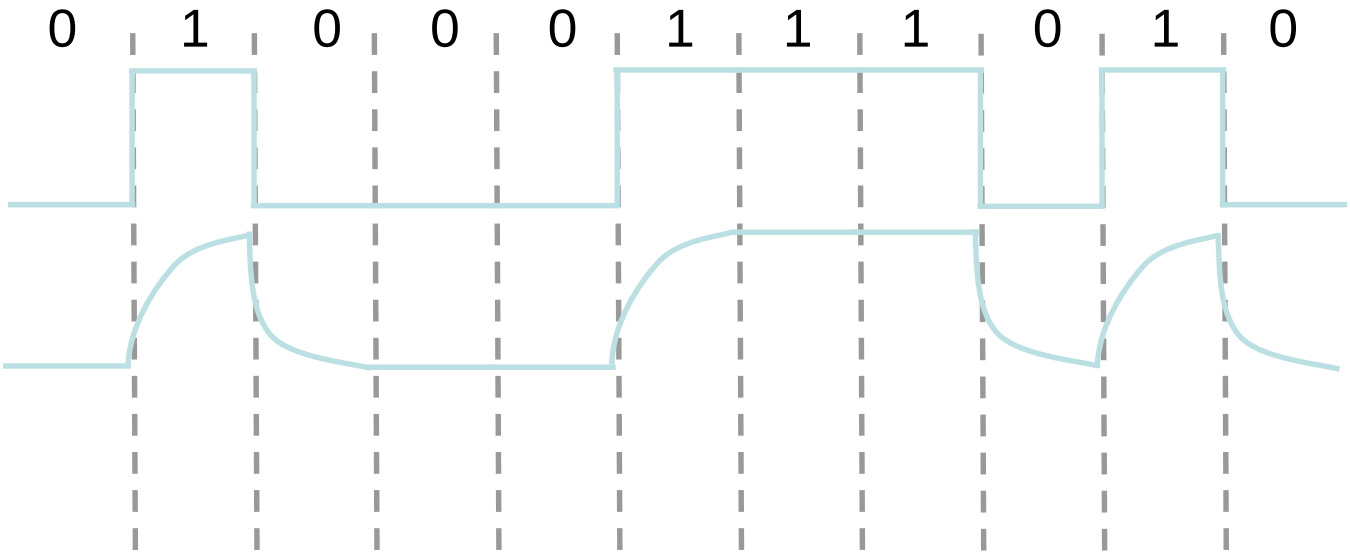




Digital Links

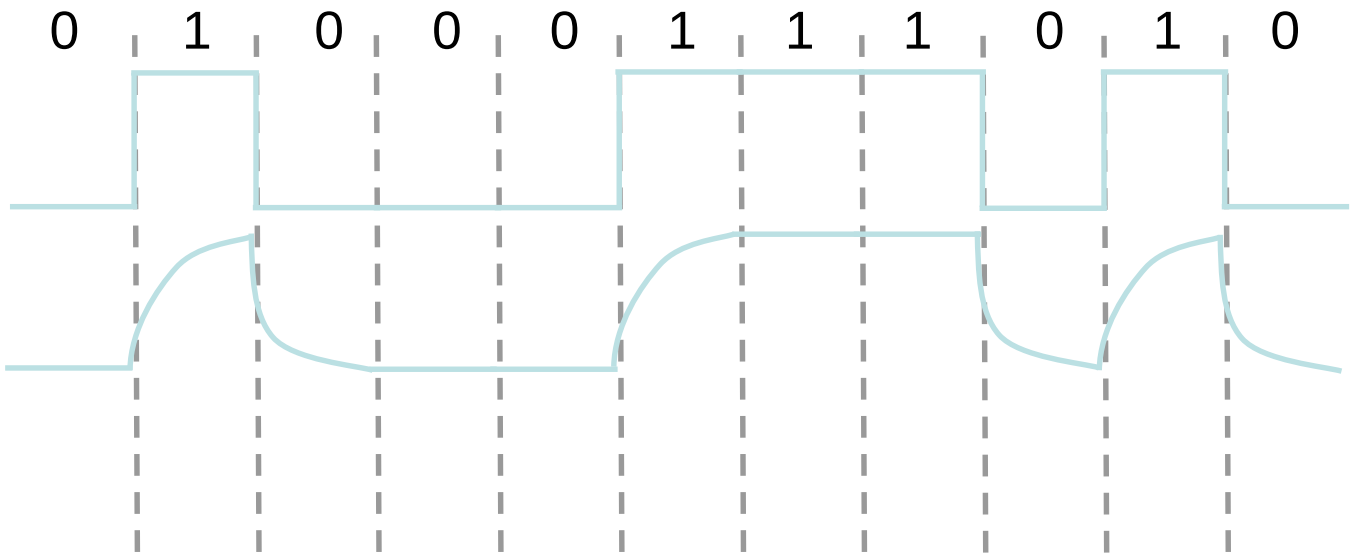
- **In ALL digital systems such as PC**
  - **All communication between ICs are digital**





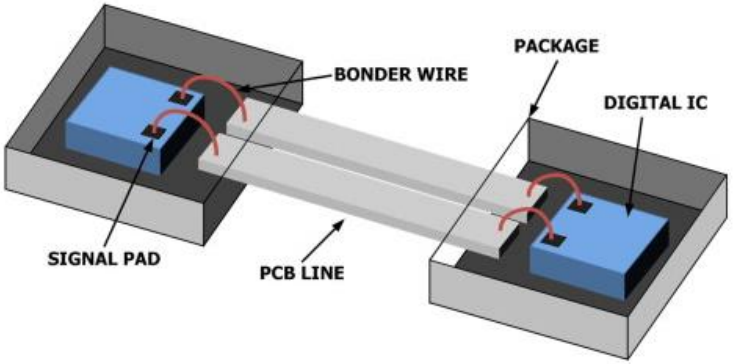
Digital Links

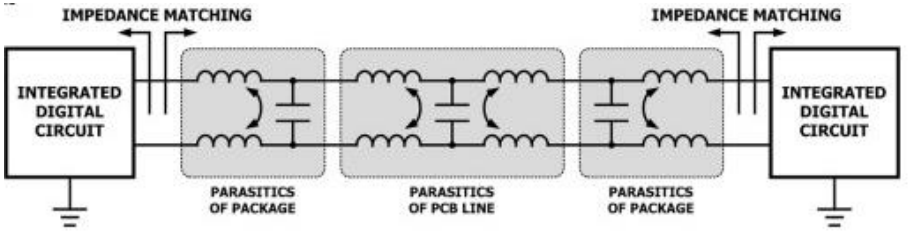
- **In ALL digital systems such as PC**
  - **All communication between ICs are digital**

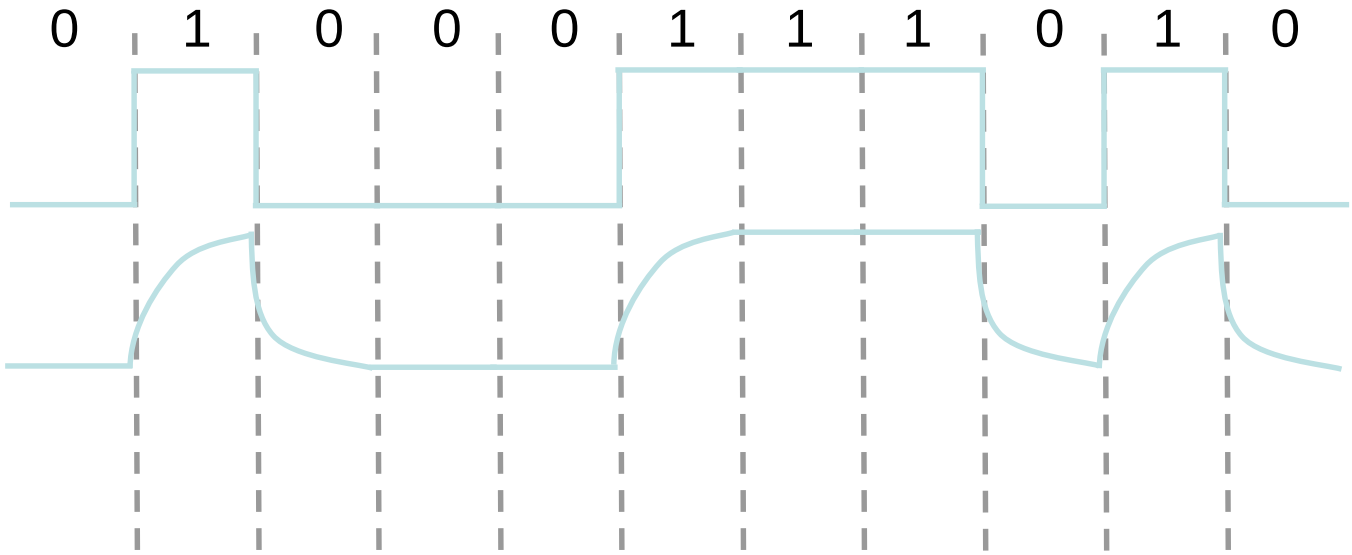


Digital Links

- **In ALL digital systems such as PC**
  - **All communication between ICs are digital**

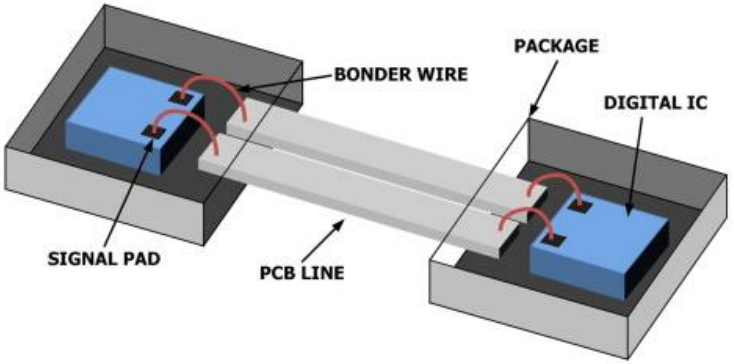


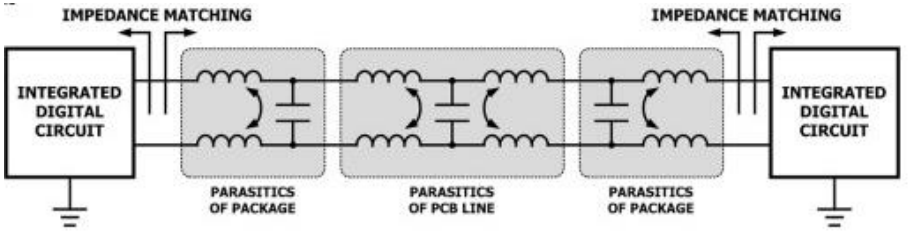


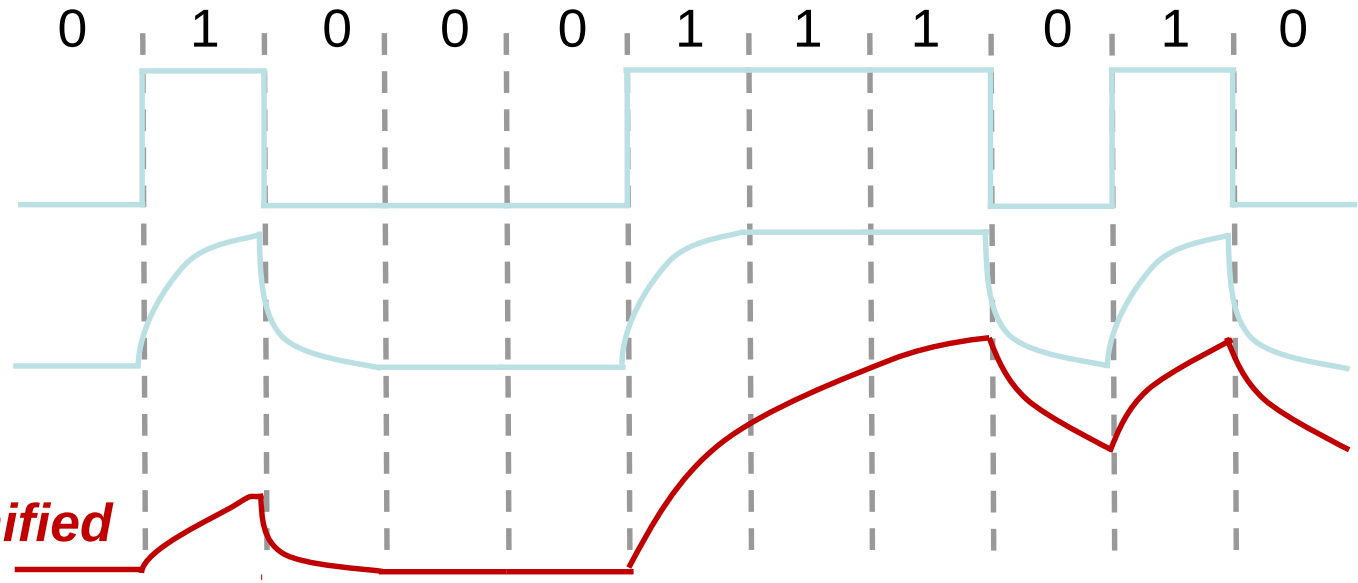


Digital Links

- **In ALL digital systems such as PC**
  - **All communication between ICs are digital**

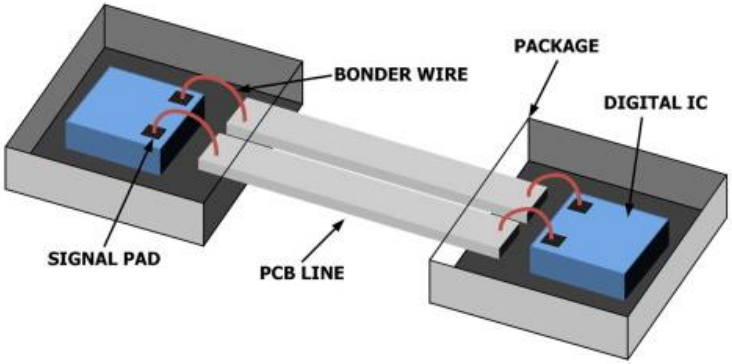


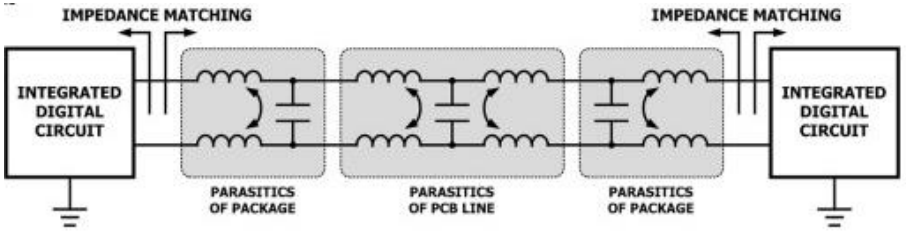


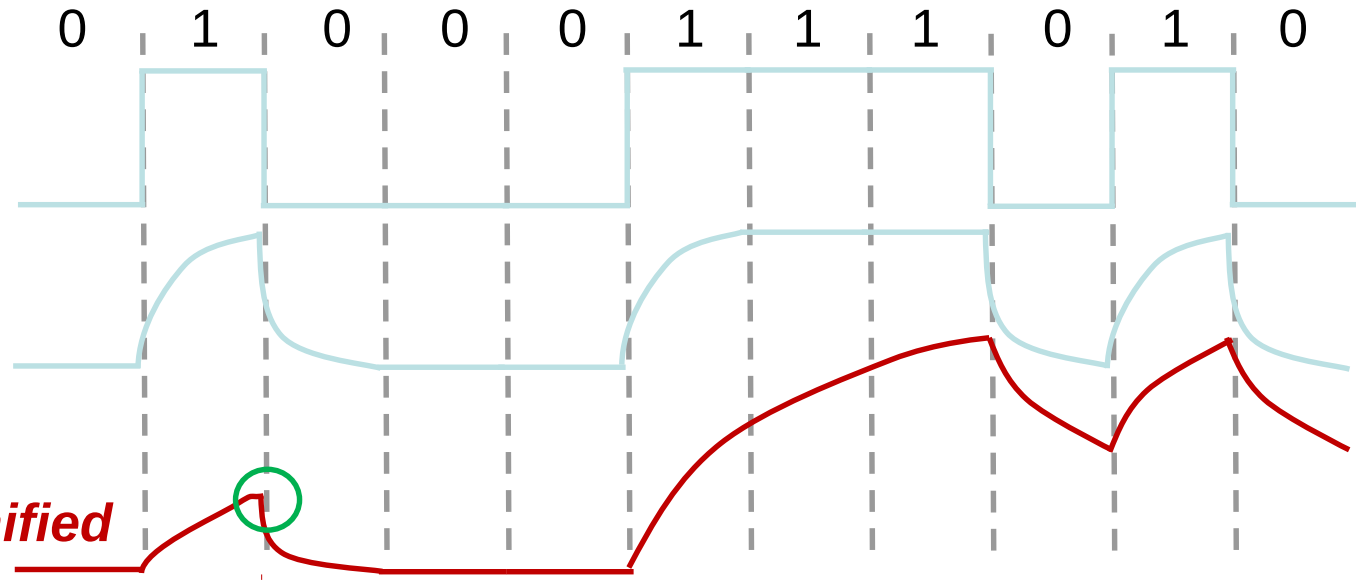


Digital Links

- **In ALL digital systems such as PC**
  - **All communication between ICs are digital**

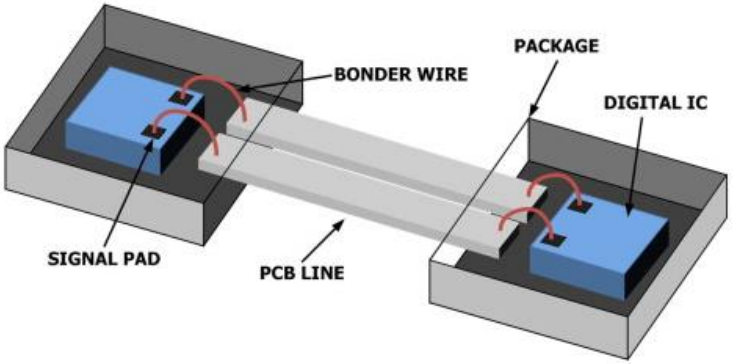


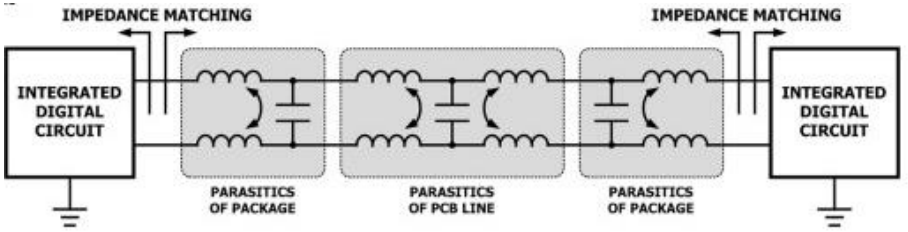


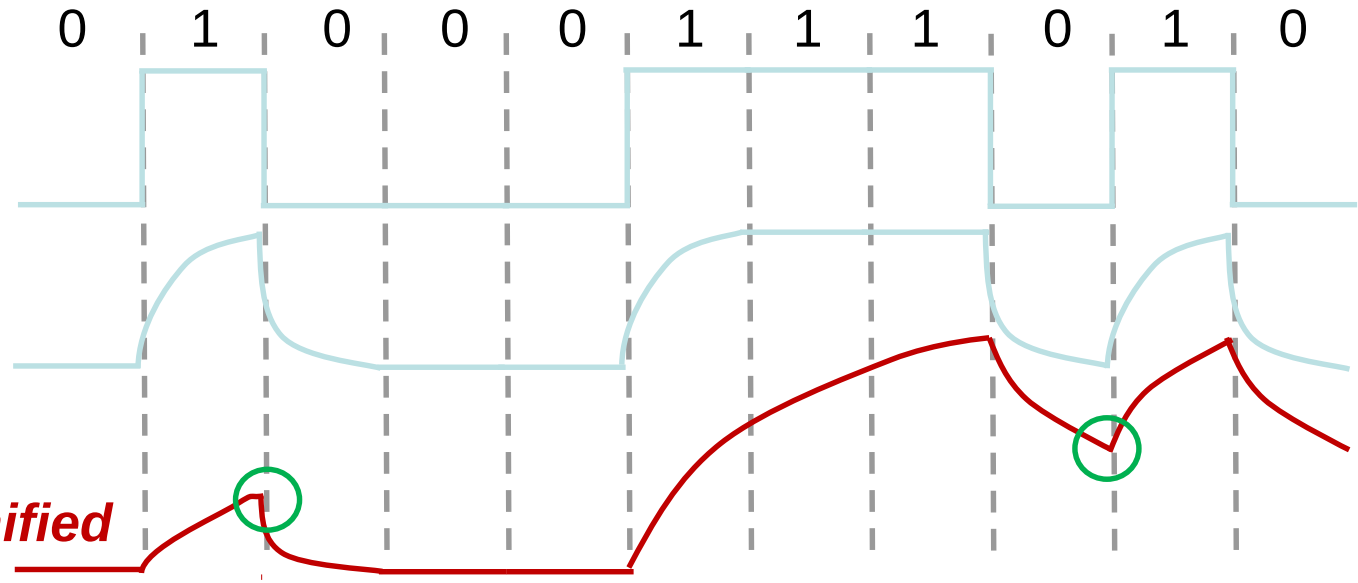


Digital Links

- **In ALL digital systems such as PC**
  - **All communication between ICs are digital**





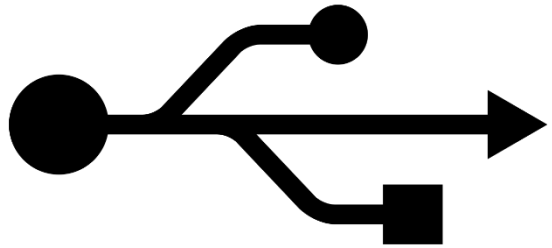


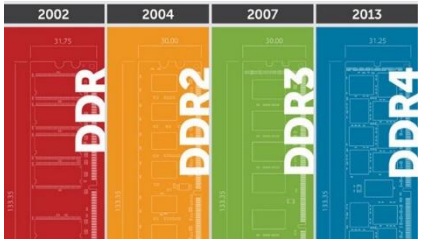
Where Else?

HDMI™
HIGH DEFINITION MULTIMEDIA INTERFACE

THUNDERBOLT™

PCI EXPRESS®





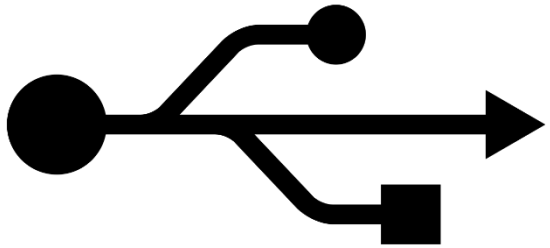
DisplayPort

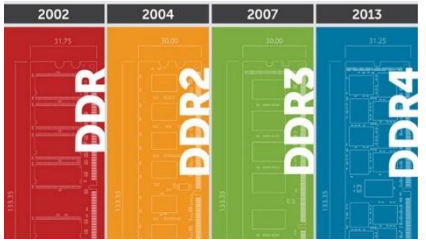
Where Else?

HDMI™ HIGH DEFINITION MULTIMEDIA INTERFACE

THUNDERBOLT™

PCI EXPRESS®



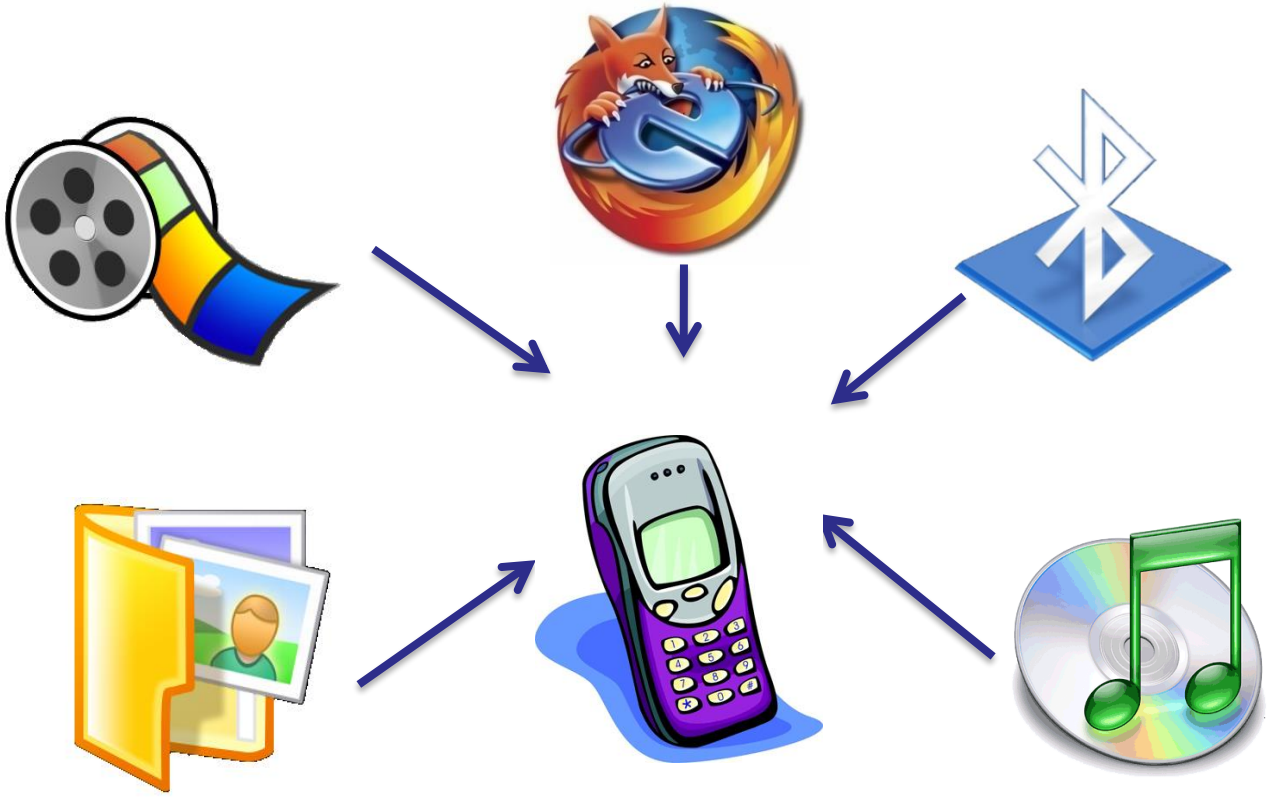


DisplayPort

- **Solutions:**
  - **Use Adaptive filtering (FIR) → Analog**
  - **Inverse Channel Filter (IIR/FIR) → Analog**
  - **High-Speed ADC (3-5 bits, >10GS/s) → Analog/Mixed-signal**

Background

- **Different applications. demand diff. specs**
  - **High bandwidth for data**
  - **High quality for audio**

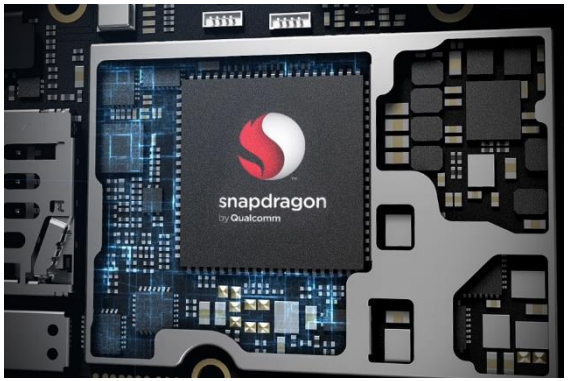


Background

- **Different applications. demand diff. specs**
  - **High bandwidth for data**
  - **High quality for audio**

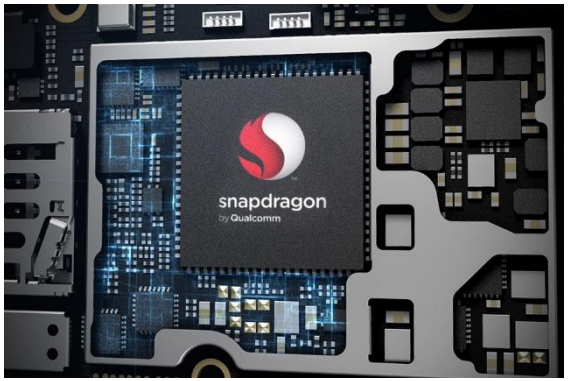
CPU/GPU and Power Management

- **Each block has AT LEAST a single power management unit**
  - **As many as 10s of PM for a single block**



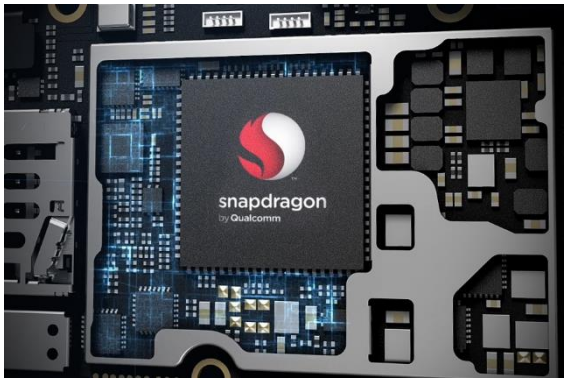
CPU/GPU and Power Management

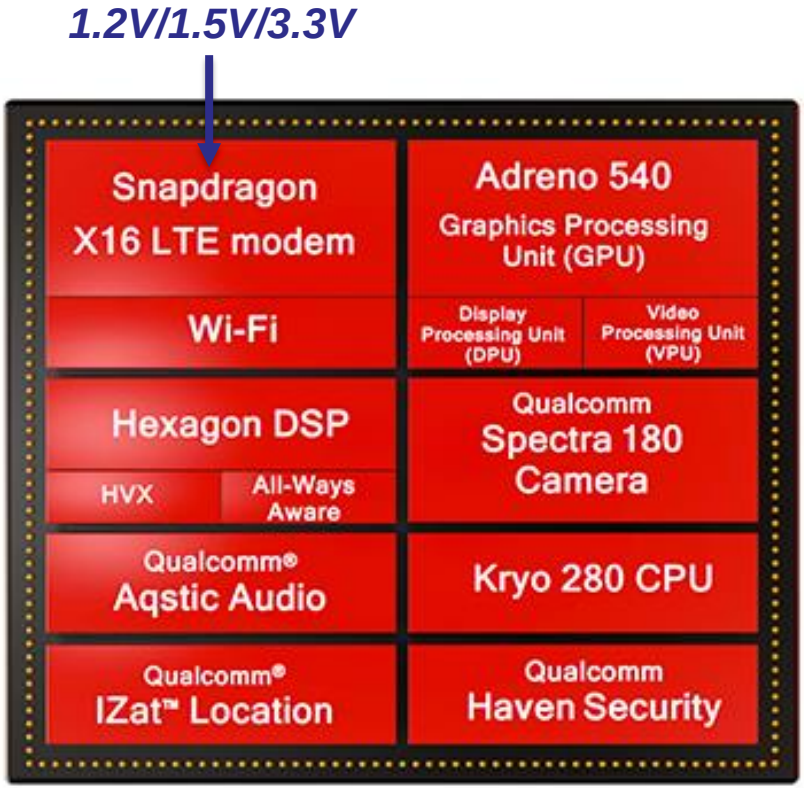
- **Each block has AT LEAST a single power management unit**
  - **As many as 10s of PM for a single block**



CPU/GPU and Power Management

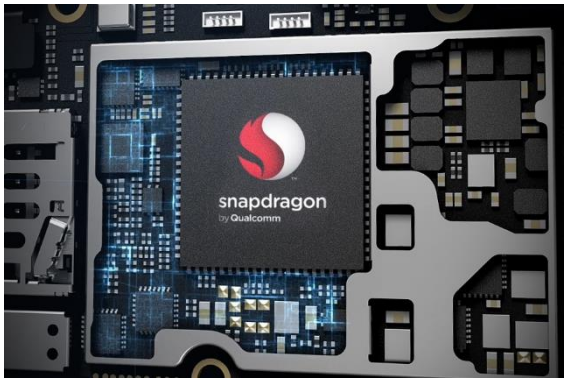
- **Each block has AT LEAST a single power management unit**
  - **As many as 10s of PM for a single block**

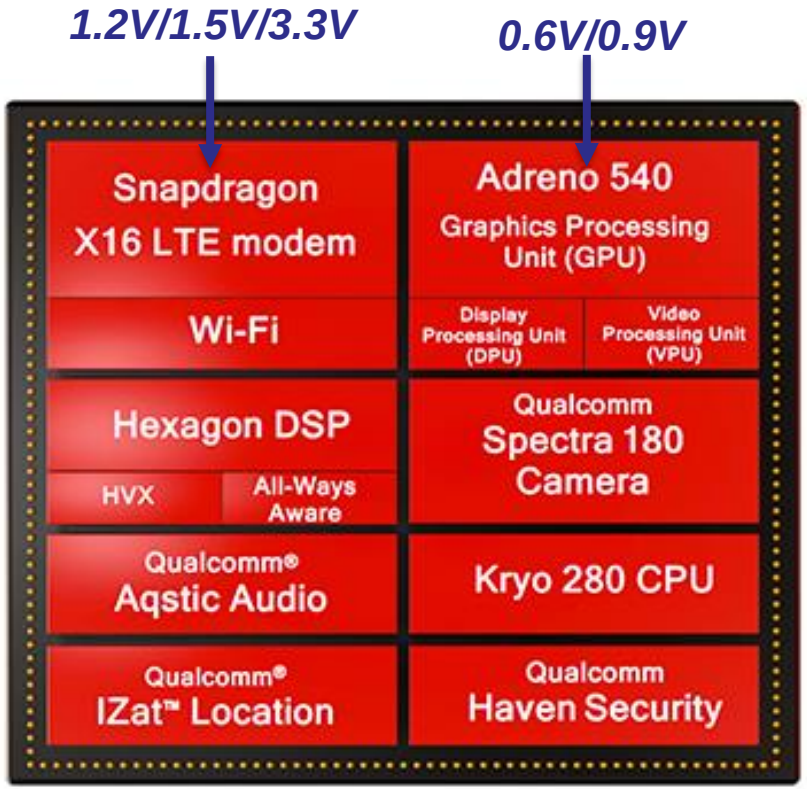




CPU/GPU and Power Management

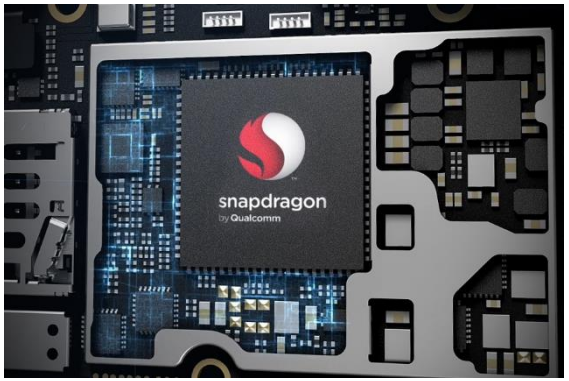
- **Each block has AT LEAST a single power management unit**
  - **As many as 10s of PM for a single block**

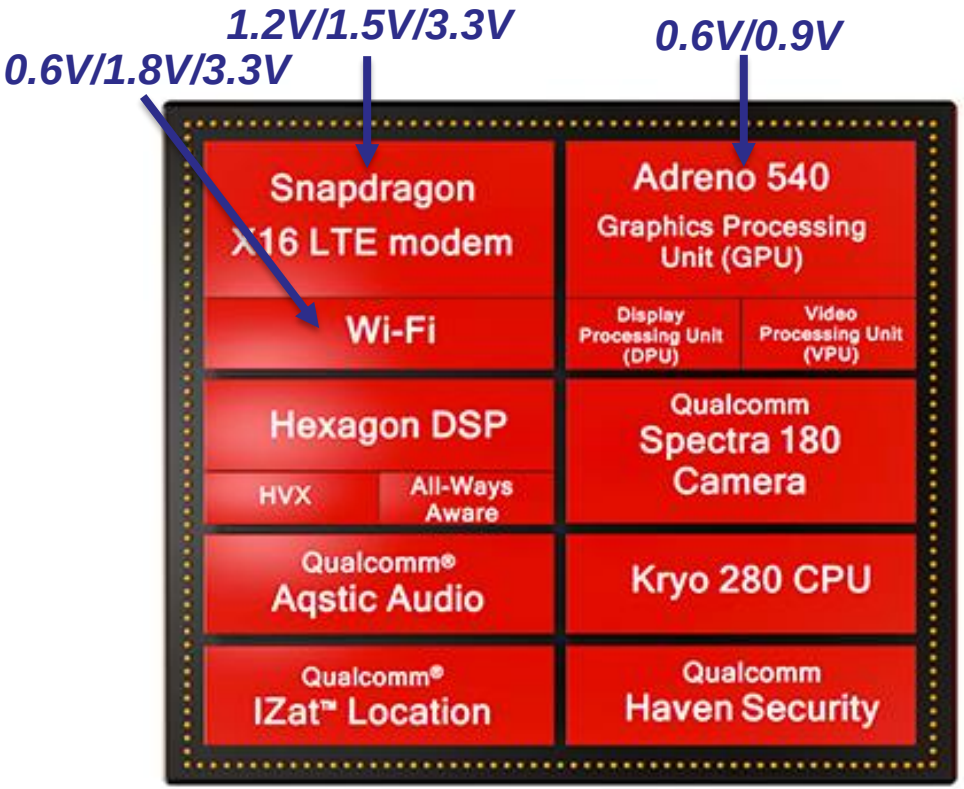




CPU/GPU and Power Management

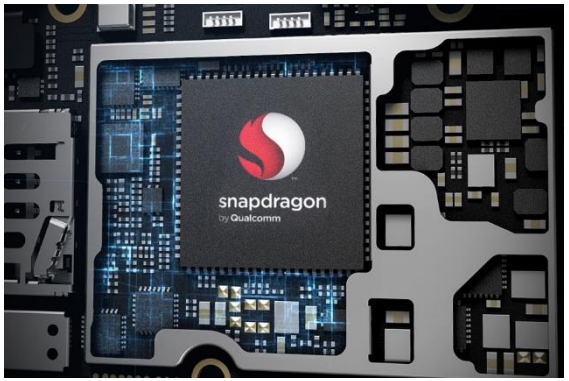
- **Each block has AT LEAST a single power management unit**
  - **As many as 10s of PM for a single block**

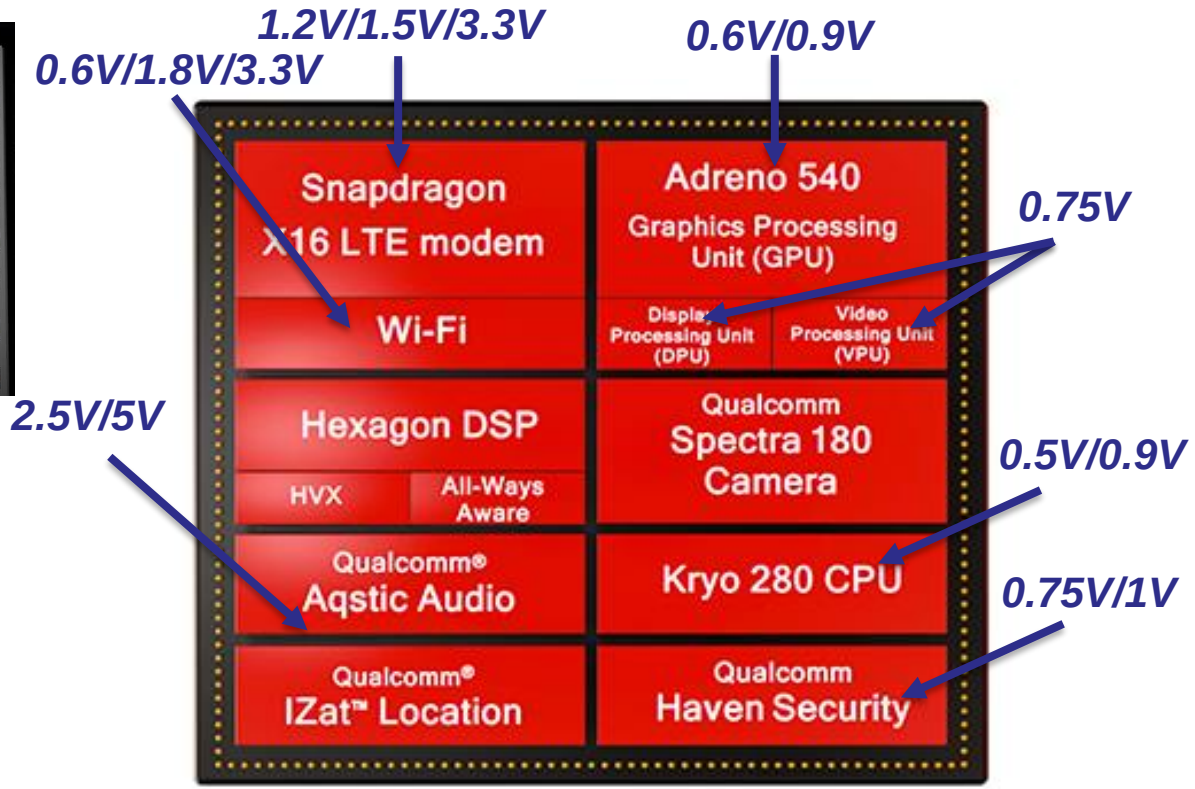




CPU/GPU and Power Management

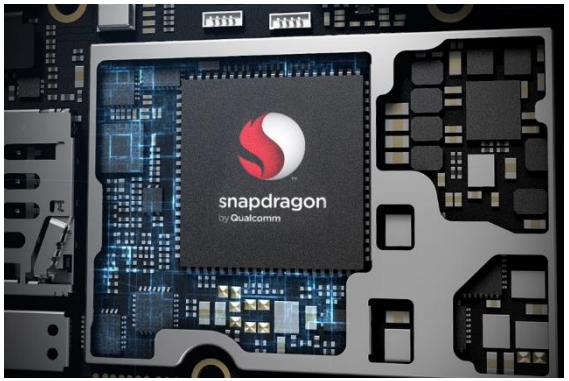
- **Each block has AT LEAST a single power management unit**
  - **As many as 10s of PM for a single block**

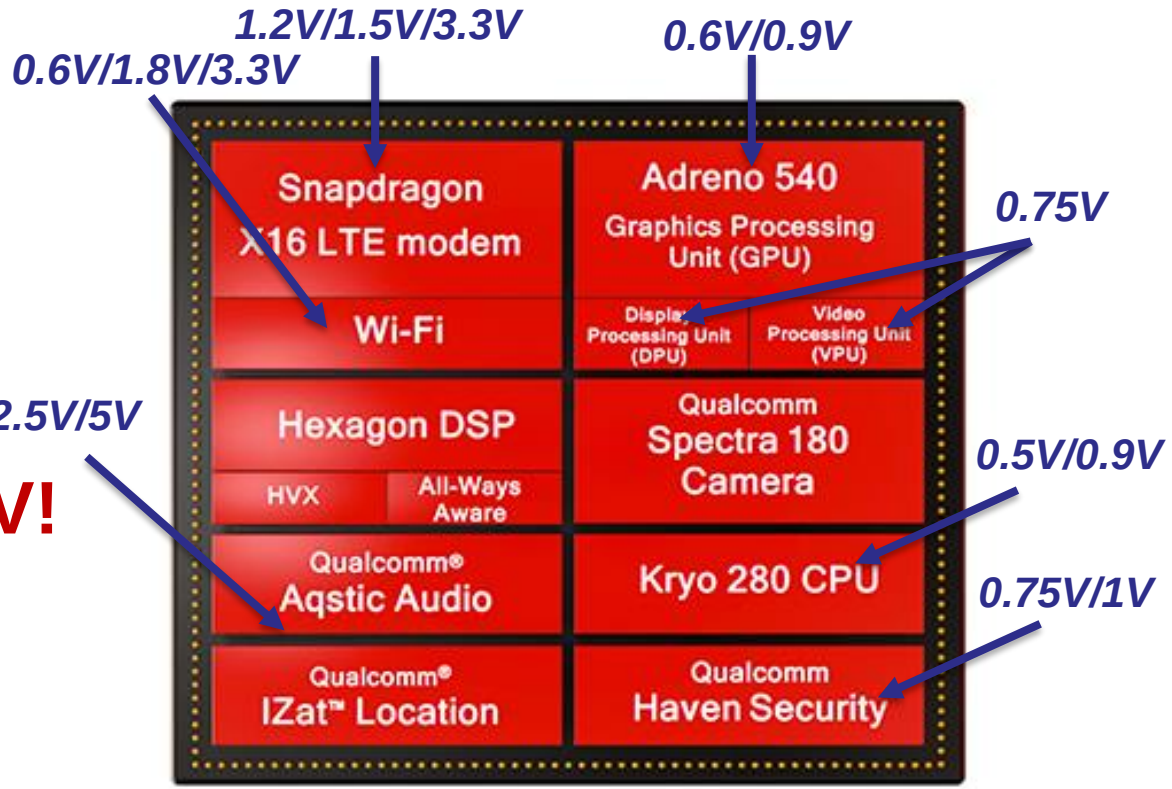




CPU/GPU and Power Management

- **Each block has AT LEAST a single power management unit**
  - **As many as 10s of PM for a single block**





Li-Ion provides 3.7V!

Summary

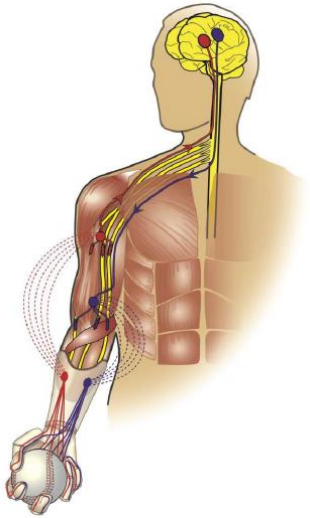
- **Analog & Mixed-Signal**

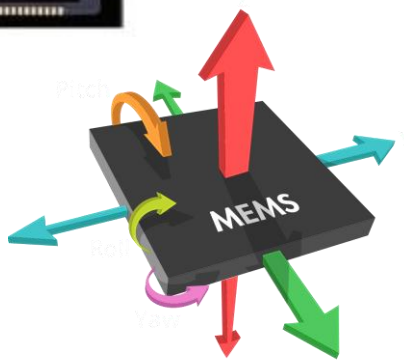
Serial Links

PCI EXPRESS®

HDMI™ HIGH DEFINITION MULTIMEDIA INTERFACE

THUNDERBOLT™





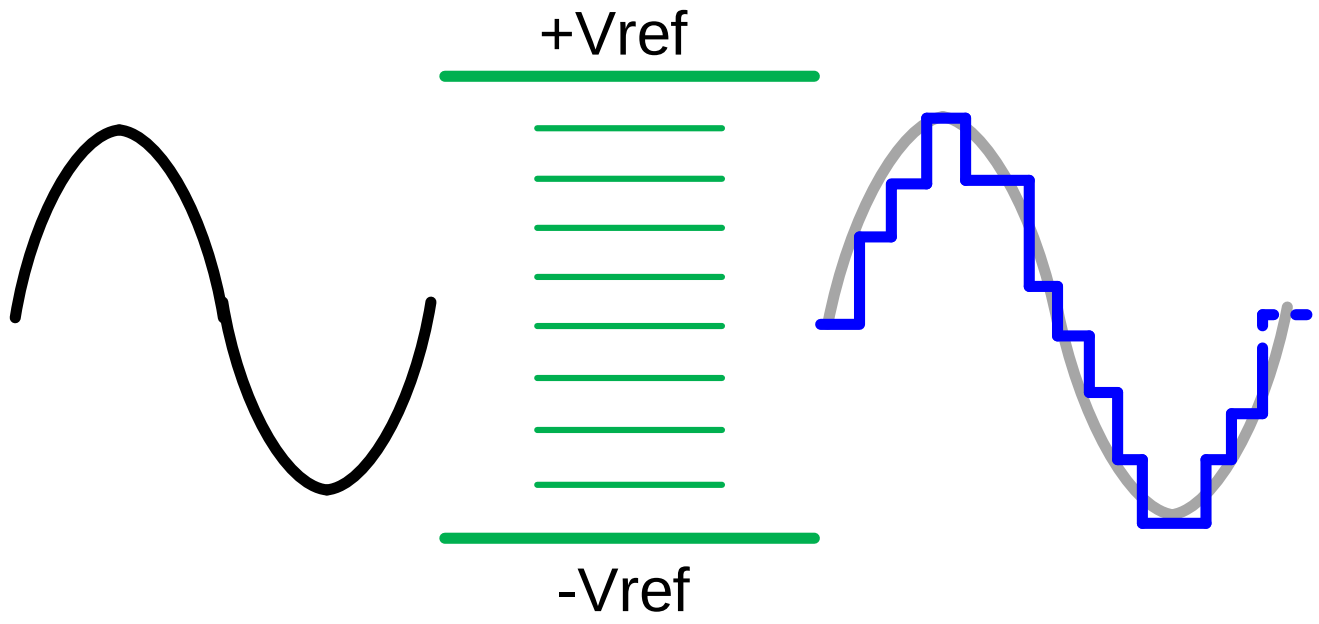
And much more….

Analog & Mixed-Signal Solutions

- **Most widely used analog & mixed signal circuits are**
  - **Analog to Digital Converters (ADCs)**
  - **Digital to Analog Converters (DACs)**
- **Broad range of speed and resolution**
- **Every SoC include many**
  - **Receiver chain**
  - **Clocking/PLL/DLLs**
  - **Power Management**
  - **Sensing & Sensor Interface**
  - **…**

Analog to Digital Conversion I

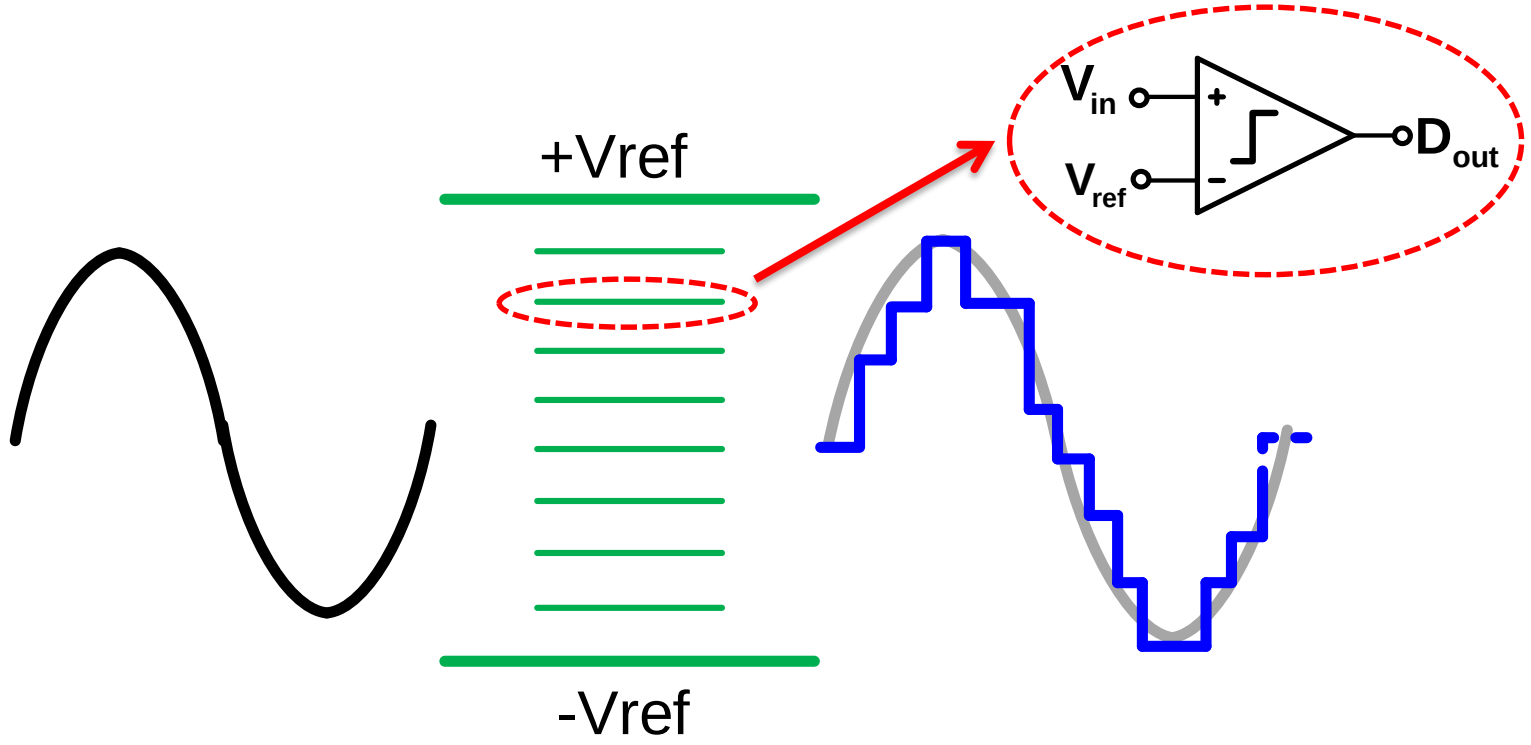
- **Human ear can detect 16-22kHz**
- **Nyquist → Sampling at 48kHz**



- **How good is the quantized sinewave?**

Analog to Digital Conversion I

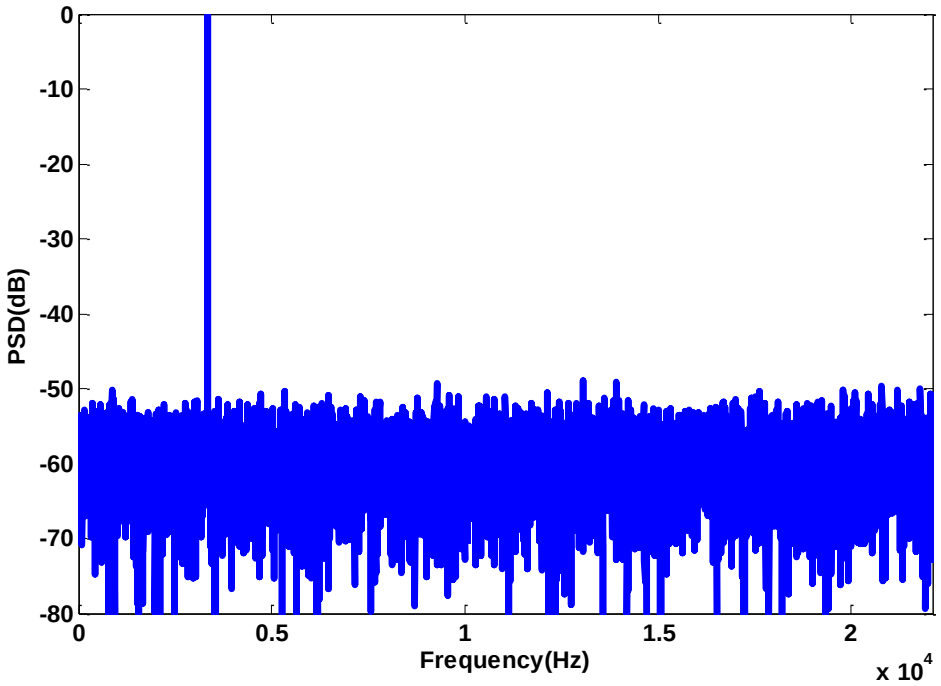
- **Human ear can detect 16-22kHz**
- **Nyquist → Sampling at 48kHz**



- **How good is the quantized sinewave?**

Analog to Digital Conversion II

- **Output spectrum (0-24kHz)**

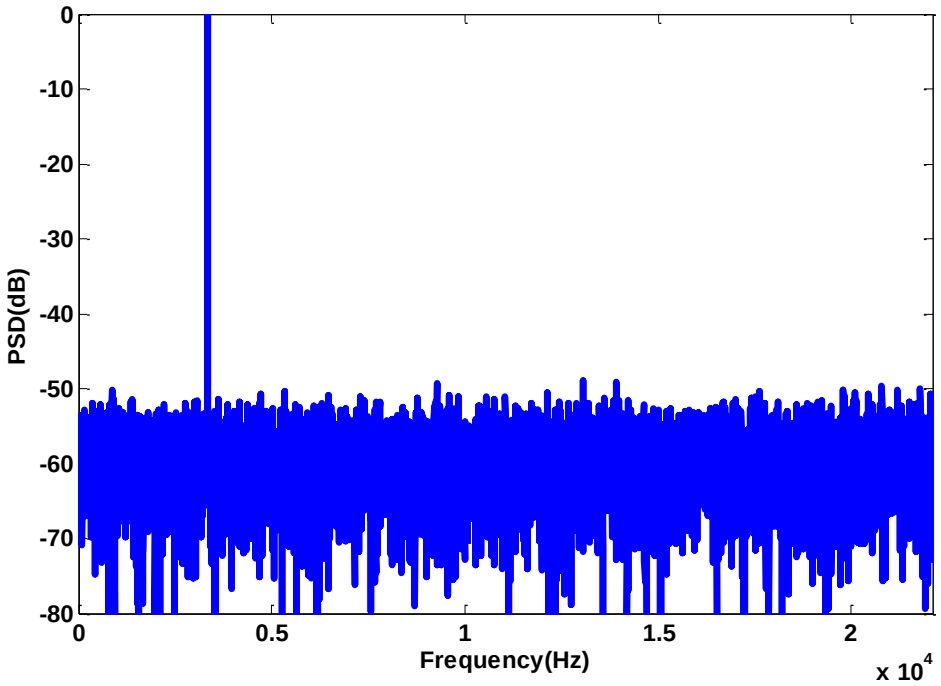


$SNR=10\log(P_{signal}/P_{noise})=20dB$

- **How many levels needed for 100dB?**

Analog to Digital Conversion II

- **Output spectrum (0-24kHz)**



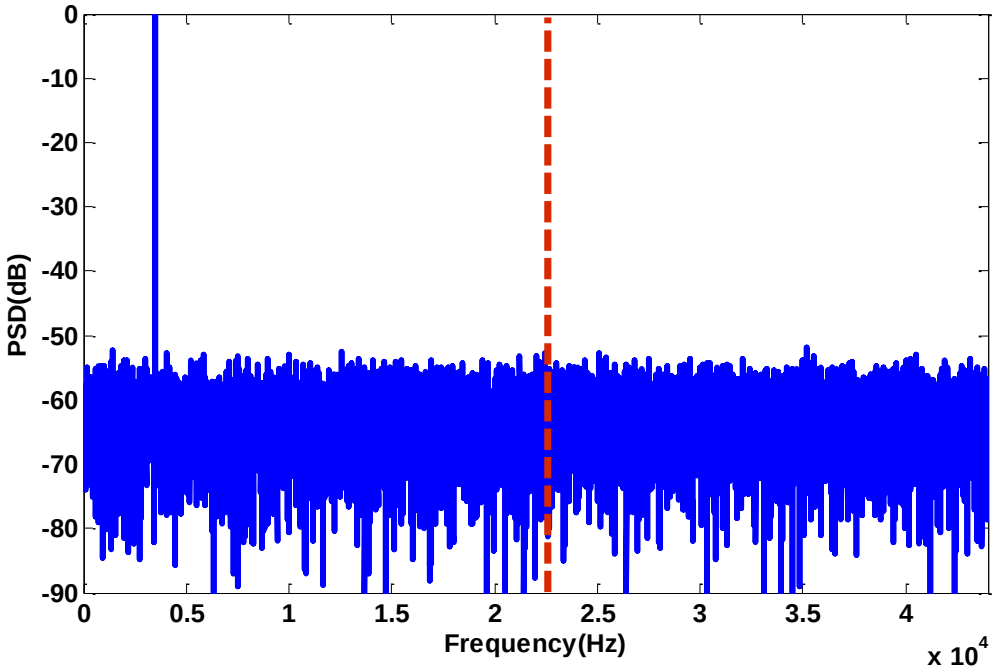
$SNR=10\log(P_{signal}/P_{noise})=20dB$

- **How many levels needed for 100dB?**

  > 65000

Oversampling

- **Sampling the signal faster (96kHz)**

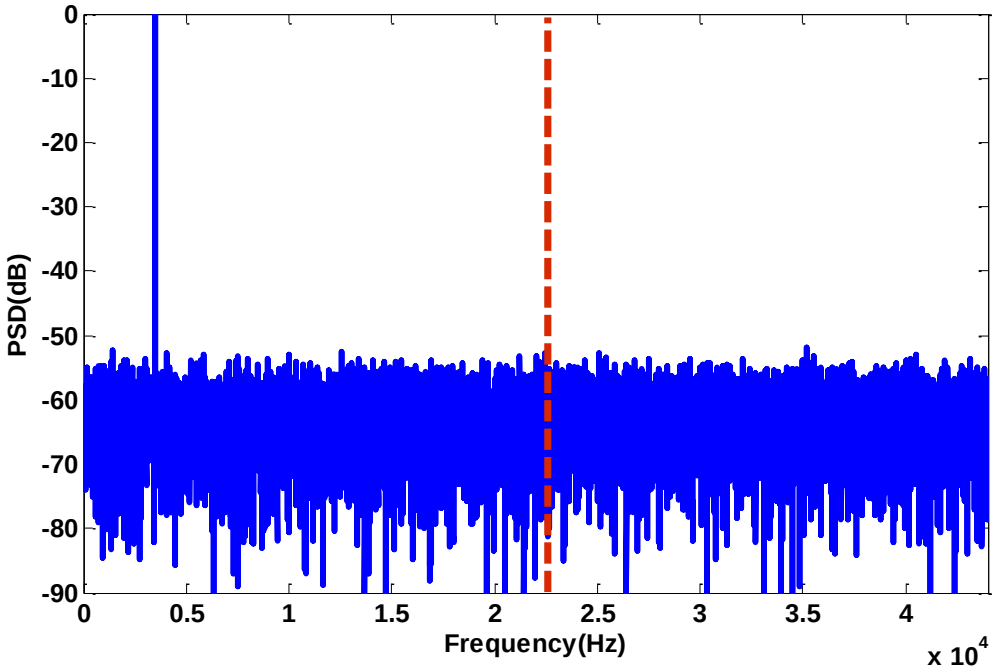


$SNR=10\log(P_{signal}/P_{noise})=23dB$

- **How much faster to get 100dB?**

Oversampling

- **Sampling the signal faster (96kHz)**



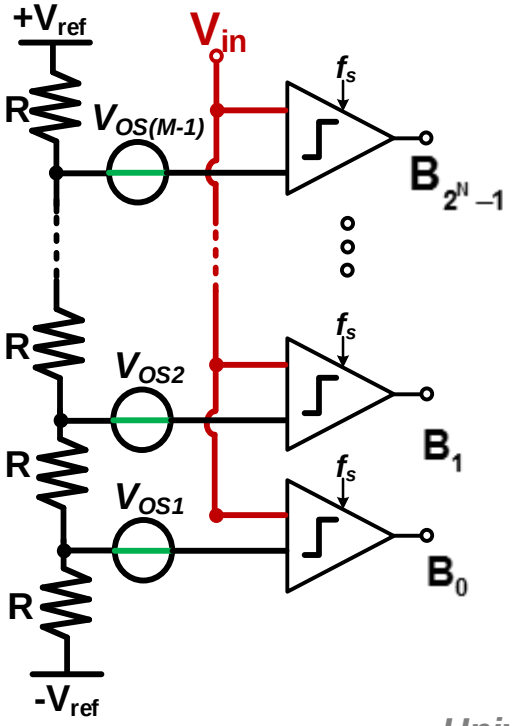
SNR=10log(P_{signal}/P_{noise})=23dB

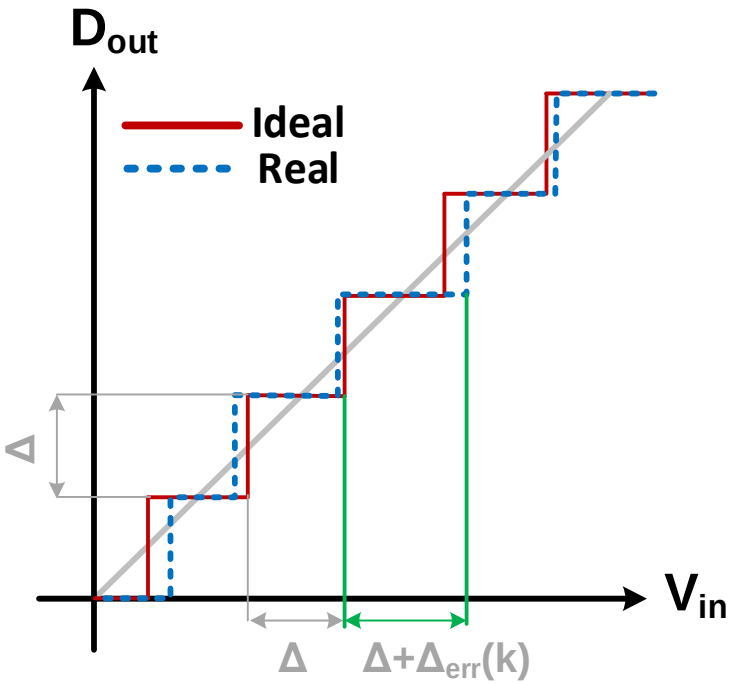
- **How much faster to get 100dB?**

  > 4.4 THz!

Flash ADC

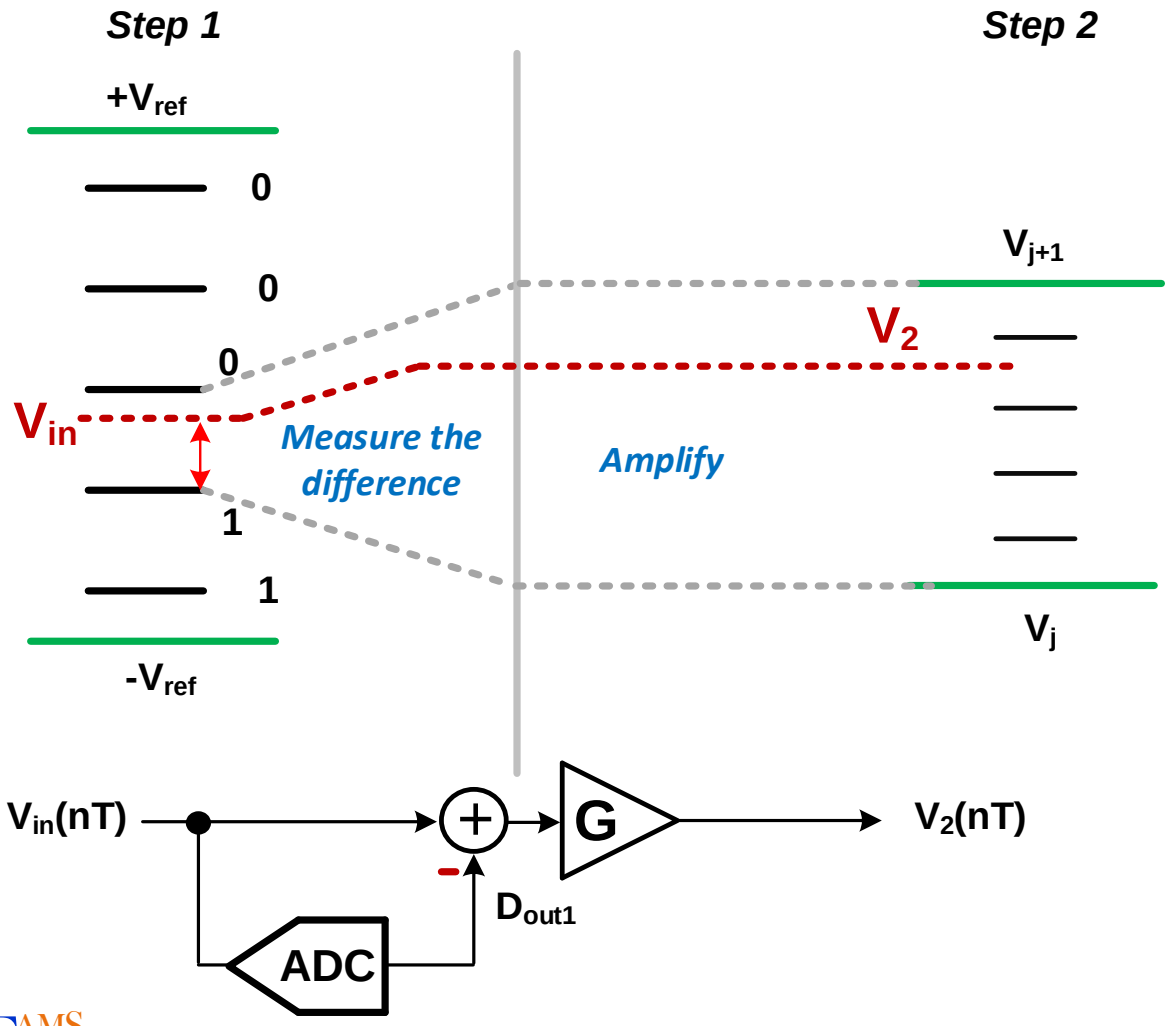
- **Fastest among all**
  - **Output is thermometer**
  - **2^N comparators are needed for N bit resolution**
  - **6-bit flash ADC requires 64 comparators**
  - **$3\sigma_{offset}$<7.5mV → not easy!**





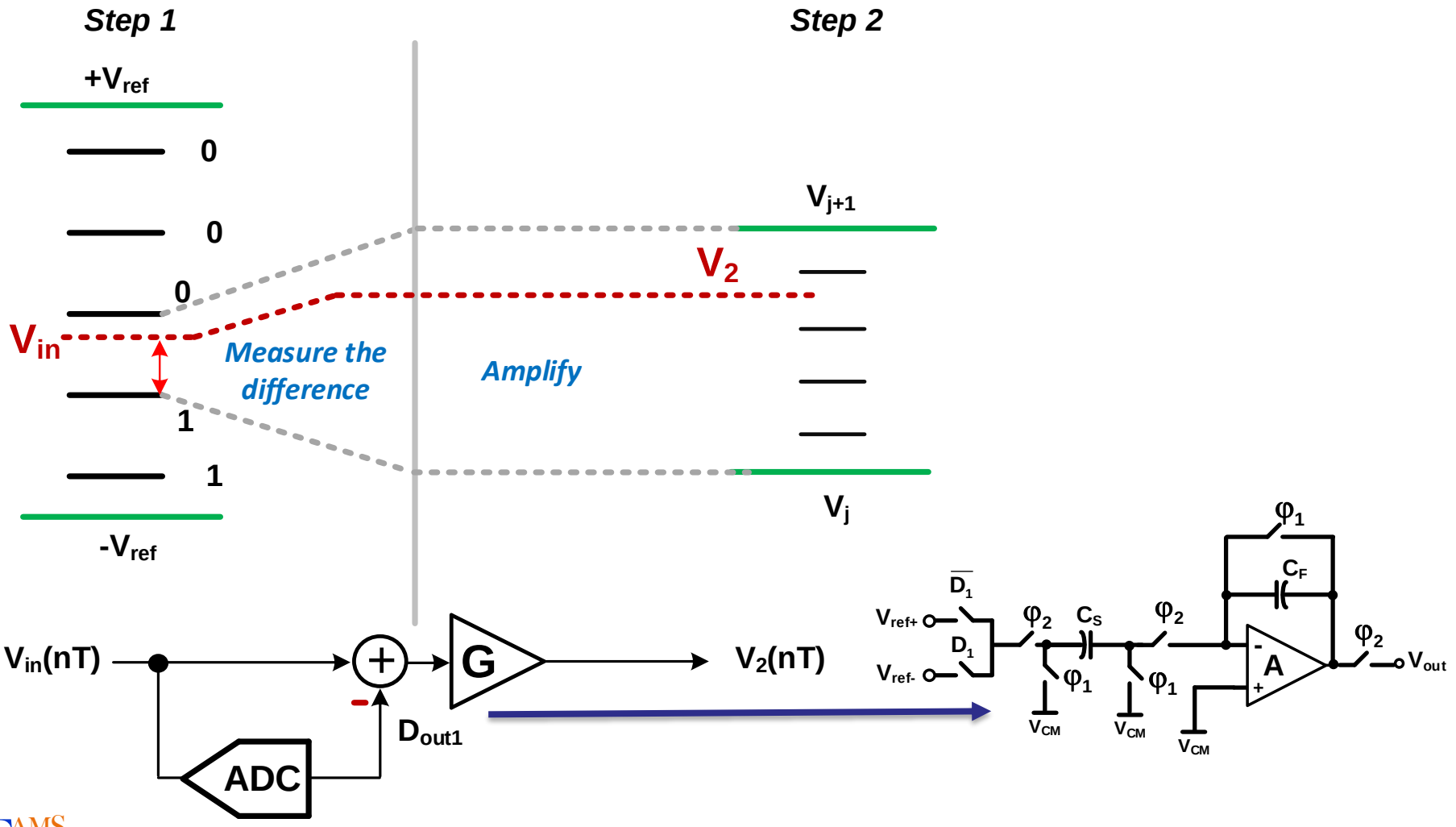
Multi-Step Concept

– Take the "Residue" of the first stage and amplify/feed it to the second stage



Multi-Step Concept

– **Take the "Residue" of the first stage and amplify/feed it to the second stage**

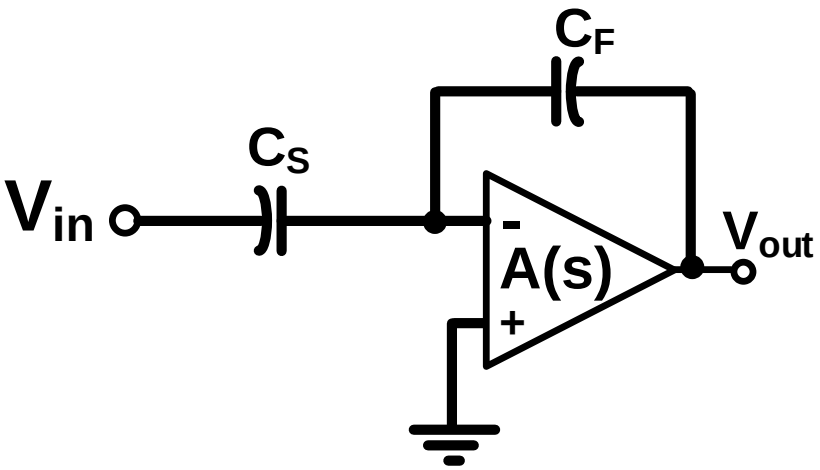


Multi-Step ADC

- **Using this approach**
  - **N bit ADC can be broken down to M+P=N bits**
  - **For instance, an 8-bit flash ADC (256 comp.)**
    - **Can be implemented using 4+4 bits**
      - **Total of 32 comparator only!**
- **The offset/noise problem is resolved**
- **For more than two decades, this was the preferred approach**

Opamp

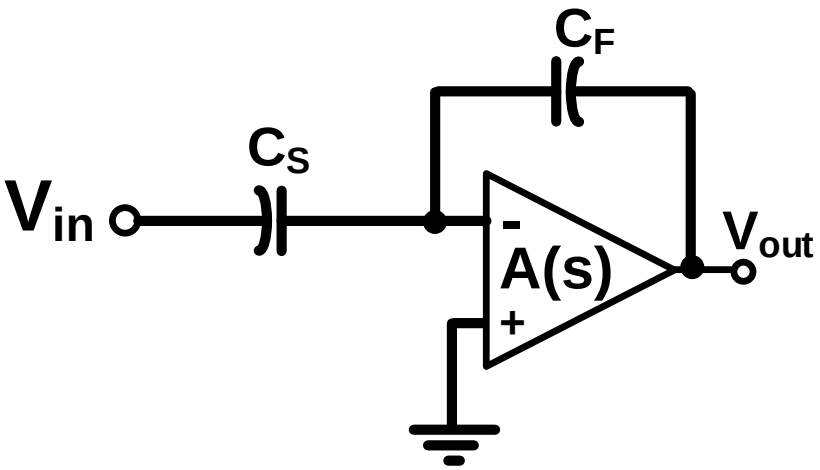
- **Amplifier**



- **For N bit ADC, the opamp should have minimum DC gain of 2^{Ntotal}**

Opamp

- **Amplifier**



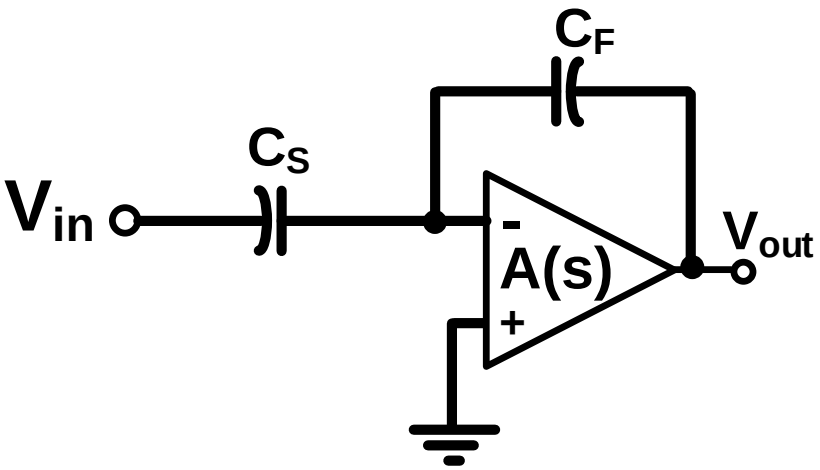
- **For N bit ADC, the opamp should have minimum DC gain of 2^{Ntotal}**

$$A_0 > 2^{N_{total}}$$

Large Gain

Opamp

- **Amplifier**



- **For N bit ADC, the opamp should have minimum DC gain of 2^{Ntotal}**
- **For sampling frequency of f_s, the BW of opamp should be**

$$A_0 > 2^{N_{total}}$$

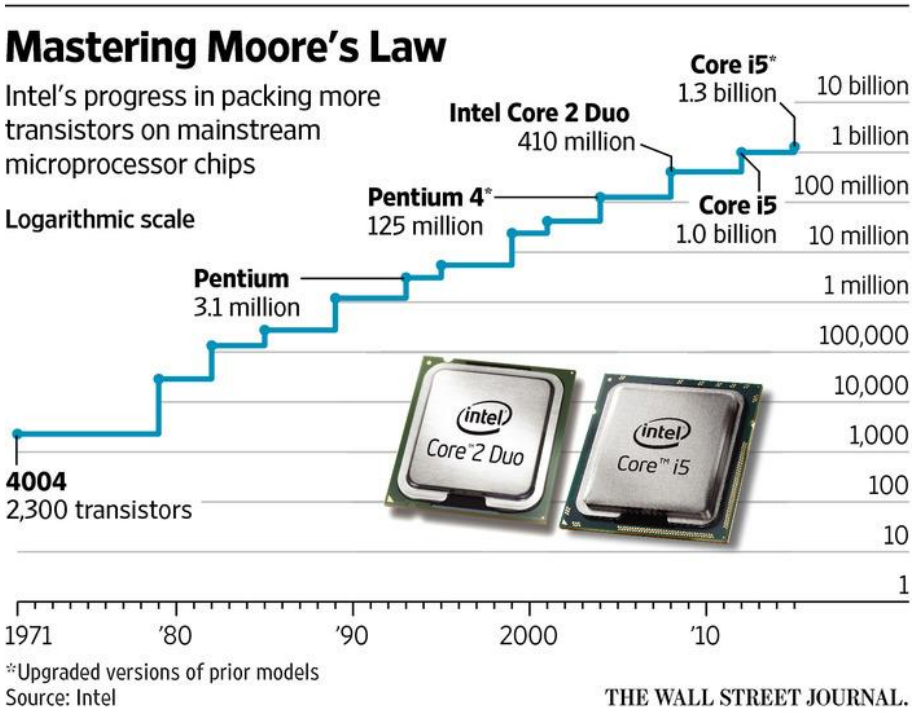
Large Gain

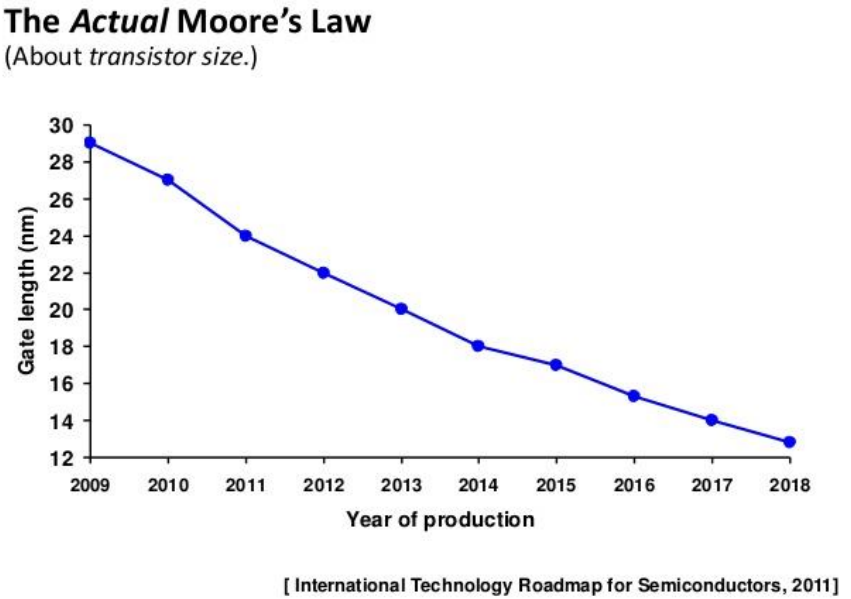
$$f_{3dB} > \frac{(N+1)}{\pi} \ln(2) \times f_s$$

Large BW

Technology Scaling

- **Moore's Law & CMOS process scaling**
  - **Double transistor count each 18 months**

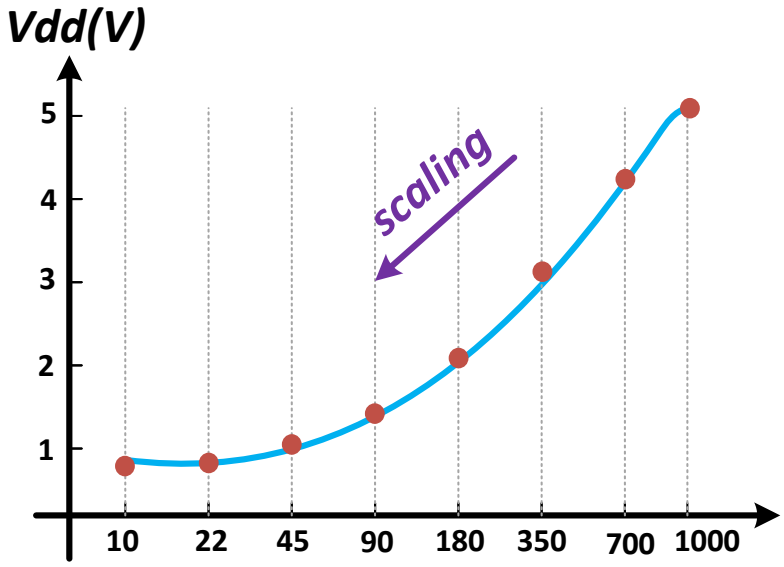


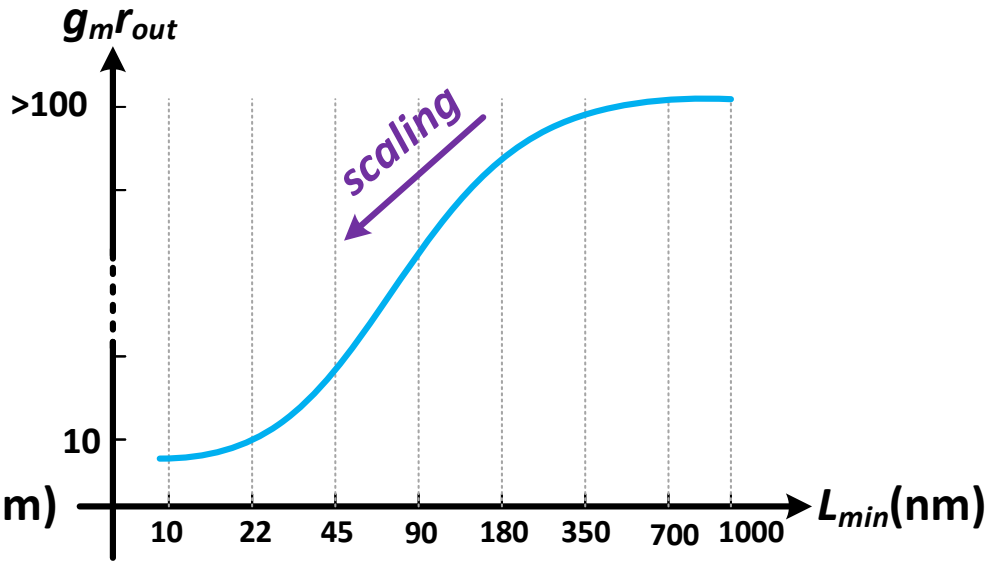


[International Technology Roadmap for Semiconductors, 2011]

Technology Scaling

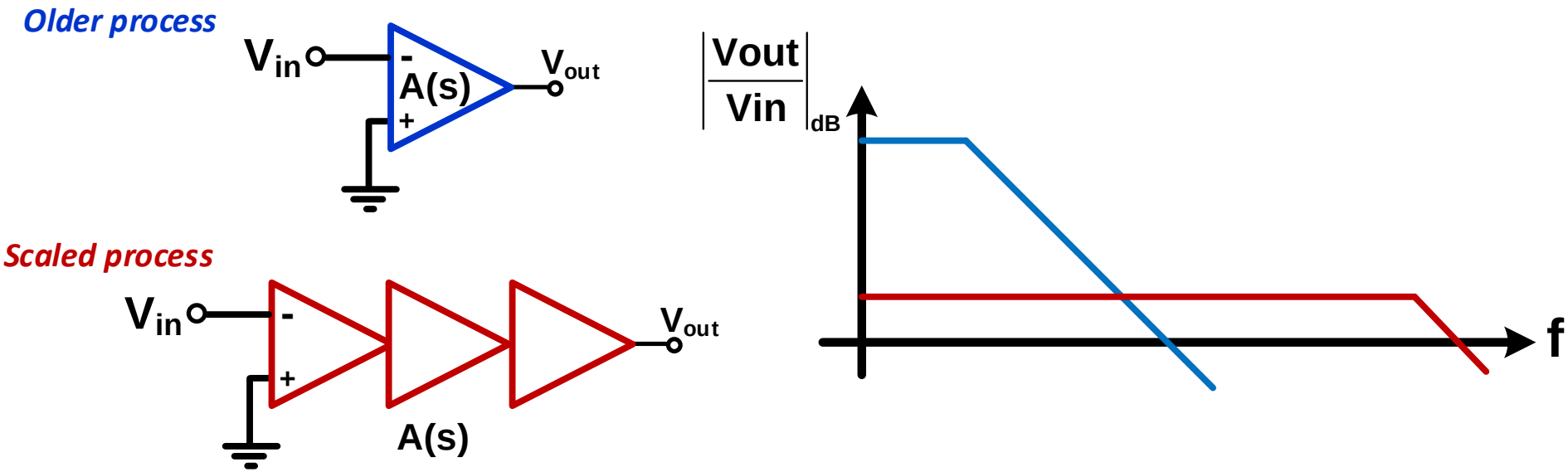
- **Moore's Law & CMOS process scaling**
  - **Double transistor count each 18 months**
  - **In terms of Analog performance & scaling**





Technology Scaling

- **Moore's Law & CMOS process scaling**
  - Transistors are becoming smaller & faster
  - Lower power, smaller area
  - Allows better integration
- **In context of analog**
  - Faster speed, but …



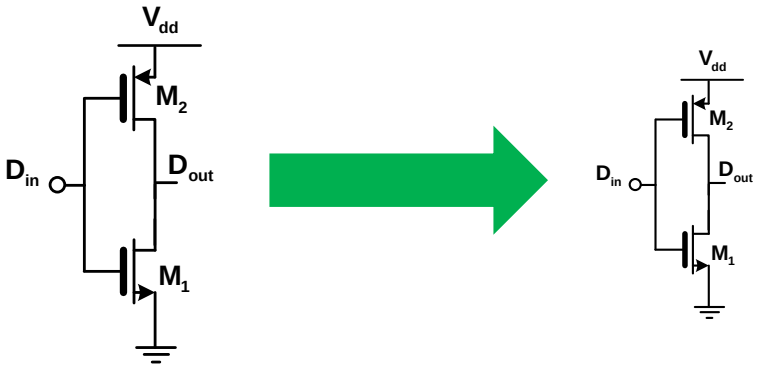
Analog Scaling

- **Digital scales *directly* in terms of**
  - **Speed**
  - **Area**
  - **Power**

- **Analog**
  - **Matching**
  - **Switching speed**
  - **Dynamic range**
  - **Noise**
  - **Area**

Analog Scaling

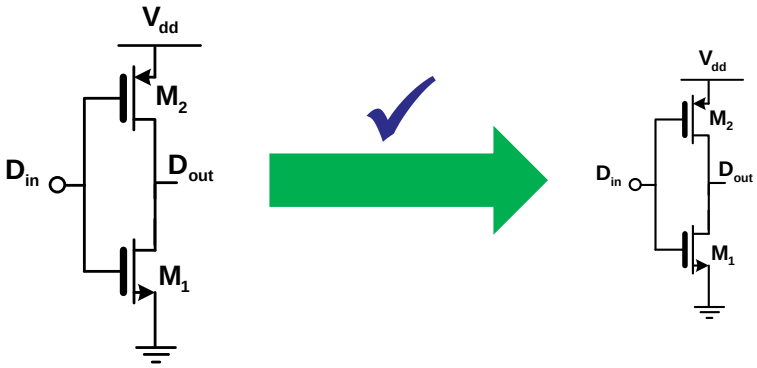
- **Digital scales *directly* in terms of**
  - **Speed**
  - **Area**
  - **Power**



- **Analog**
  - **Matching**
  - **Switching speed**
  - **Dynamic range**
  - **Noise**
  - **Area**

Analog Scaling

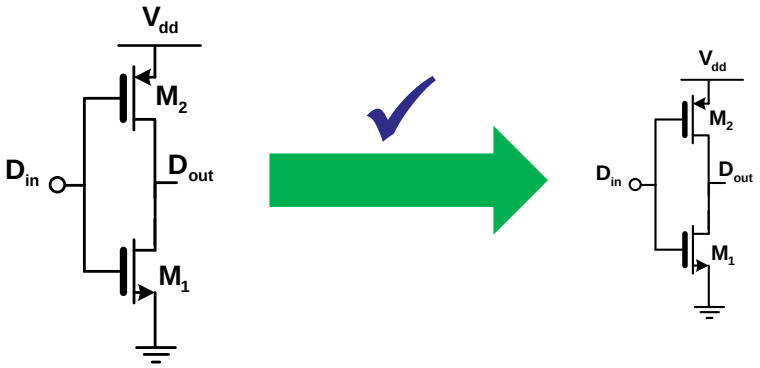
- **Digital scales *directly* in terms of**
  - **Speed**
  - **Area**
  - **Power**



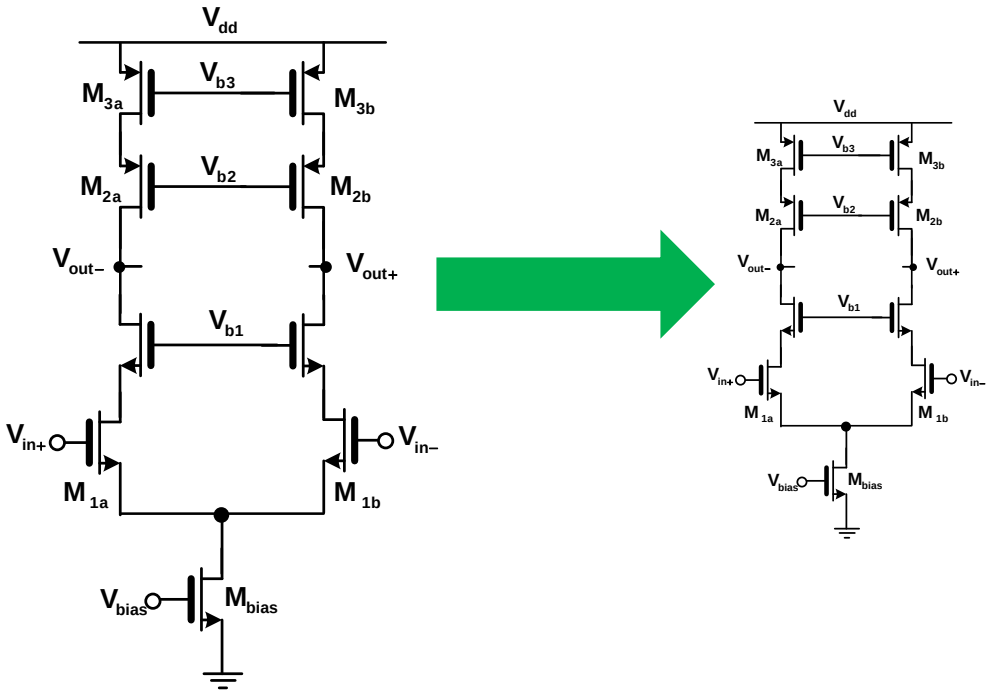
- **Analog**
  - **Matching**
  - **Switching speed**
  - **Dynamic range**
  - **Noise**
  - **Area**

Analog Scaling

- **Digital scales *directly* in terms of**
  - **Speed**
  - **Area**
  - **Power**

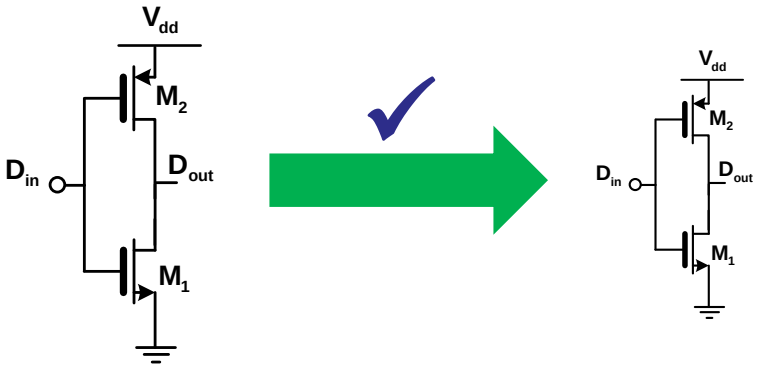


- **Analog**
  - **Matching**
  - **Switching speed**
  - **Dynamic range**
  - **Noise**
  - **Area**

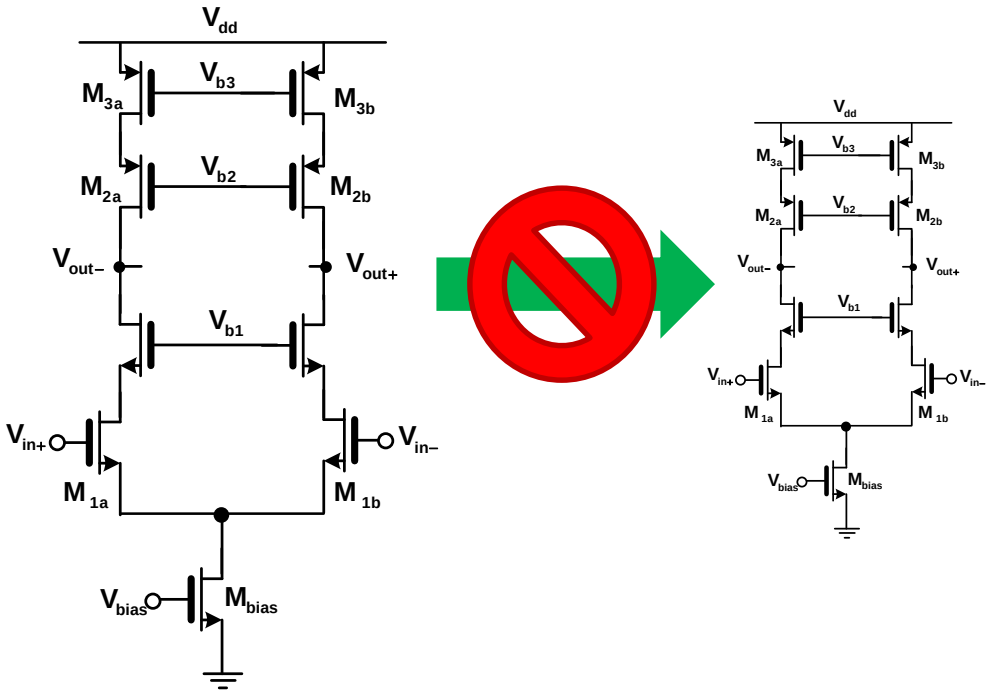


Analog Scaling

- **Digital scales *directly* in terms of**
  - **Speed**
  - **Area**
  - **Power**



- **Analog**
  - **Matching**
  - **Switching speed**
  - **Dynamic range**
  - **Noise**
  - **Area**



Analog Scaling

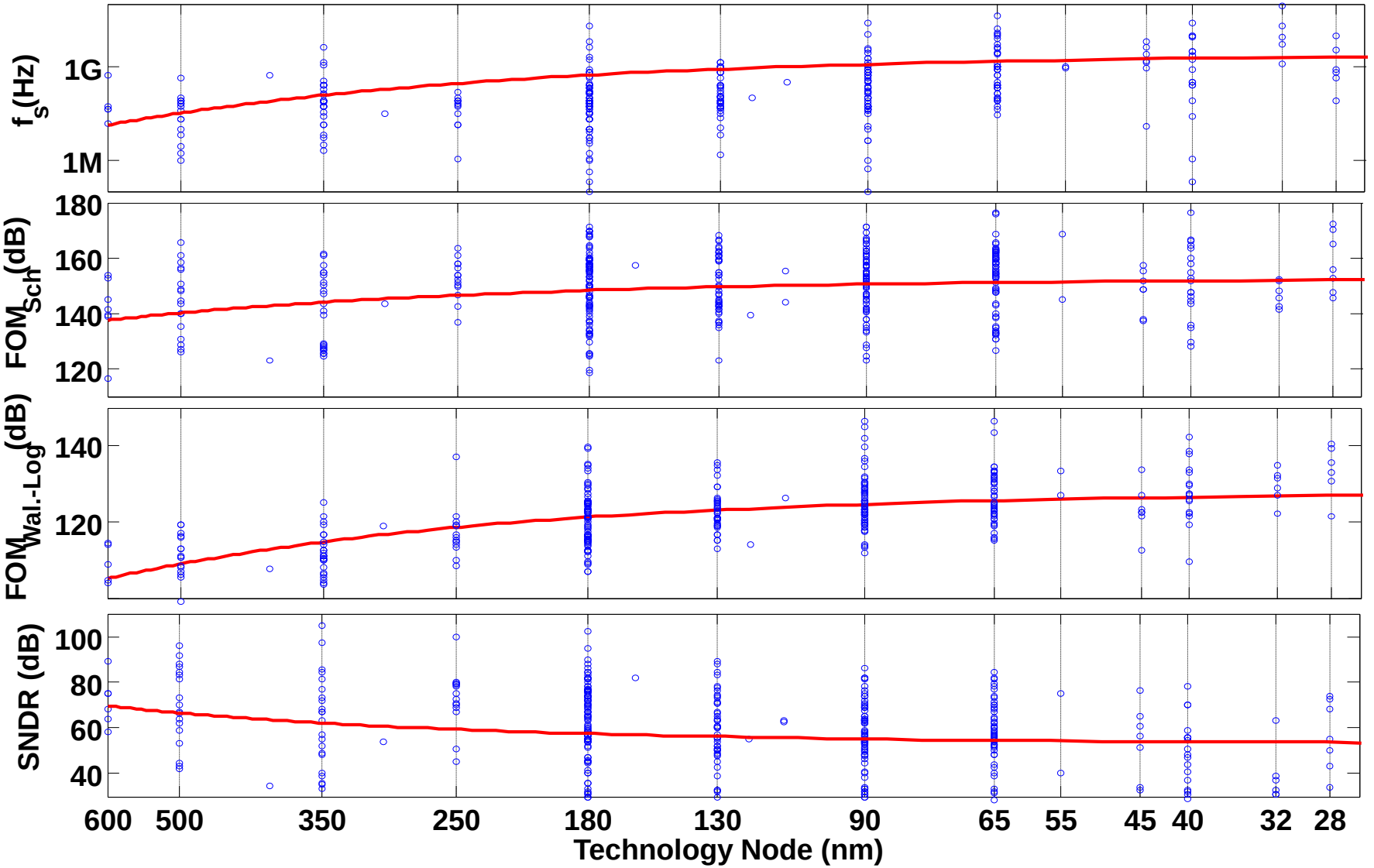
Innovative Solutions are needed To allow Analog scale well in advanced CMOS nodes

Analog Scaling

Innovative Solutions are needed To allow Analog scale well in advanced CMOS nodes

even with that …

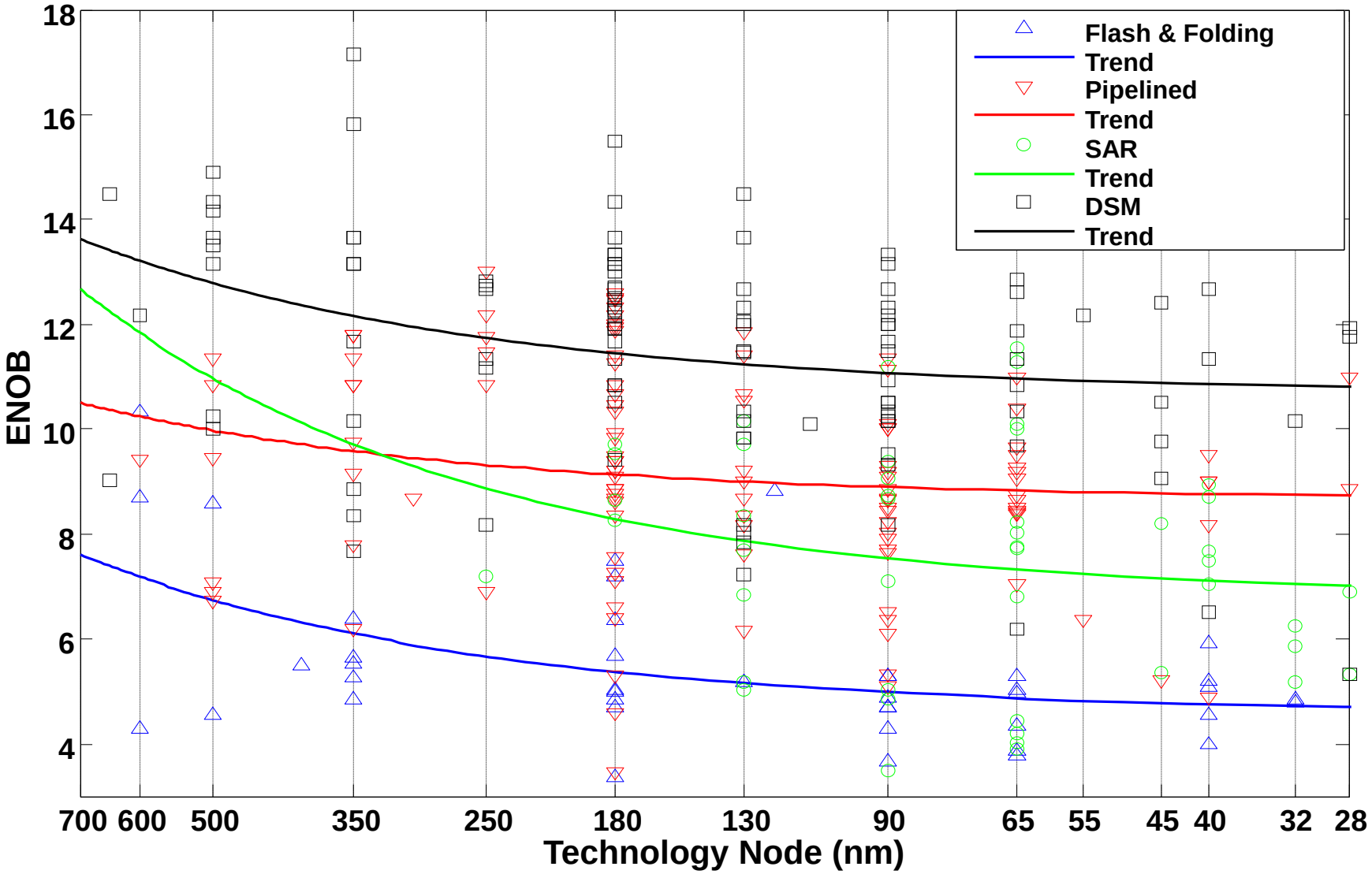
ADCs vs. Tech. node



$$FOM_{Wal\text{-}log}=10\log\left(\frac{Power}{2*BW*2^{ENOB}}\right)^{-1}$$

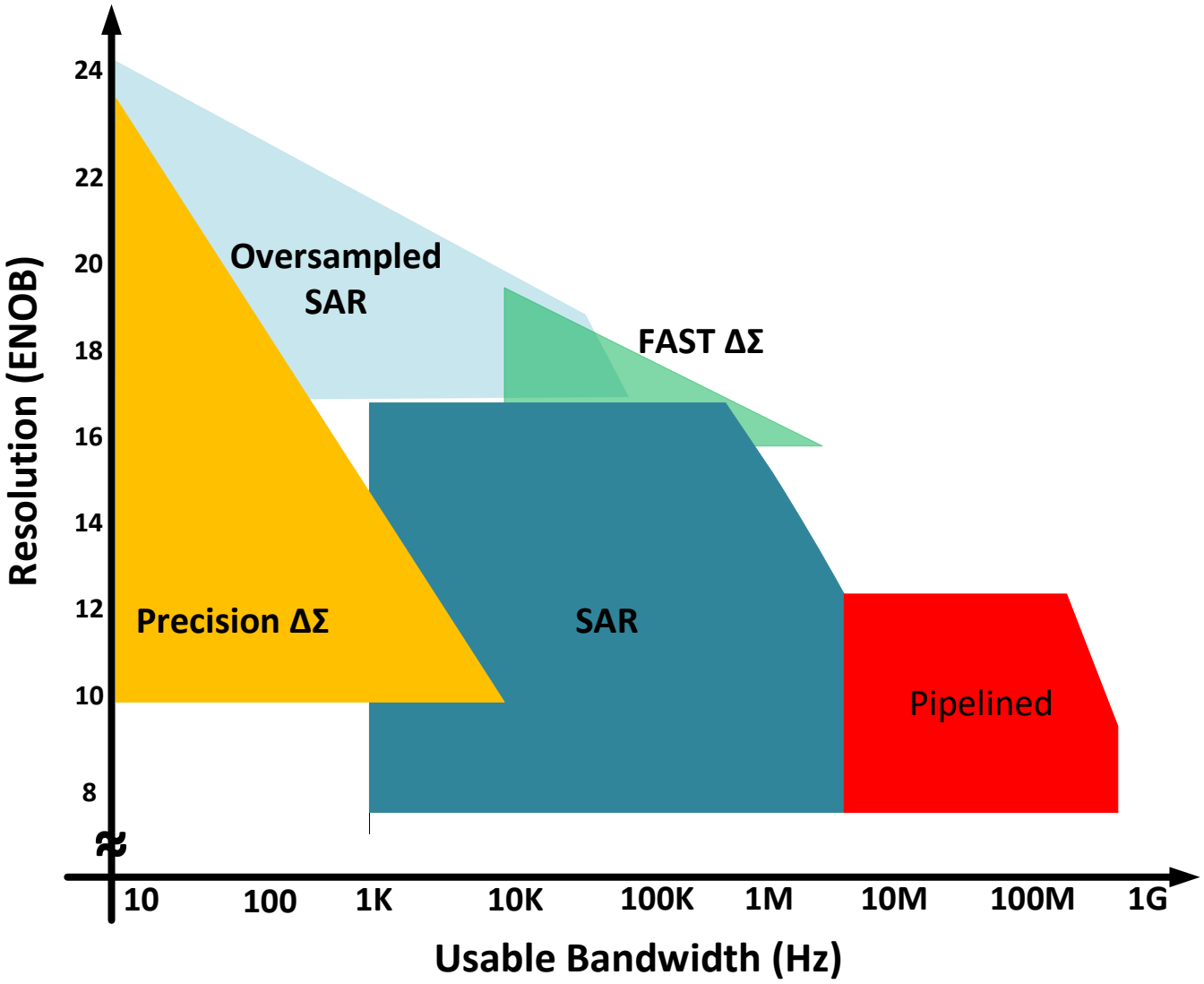
$$FOM_{Sch}=DR(dB)+10log\frac{BW}{Power}$$

ADC types vs. Tech. node



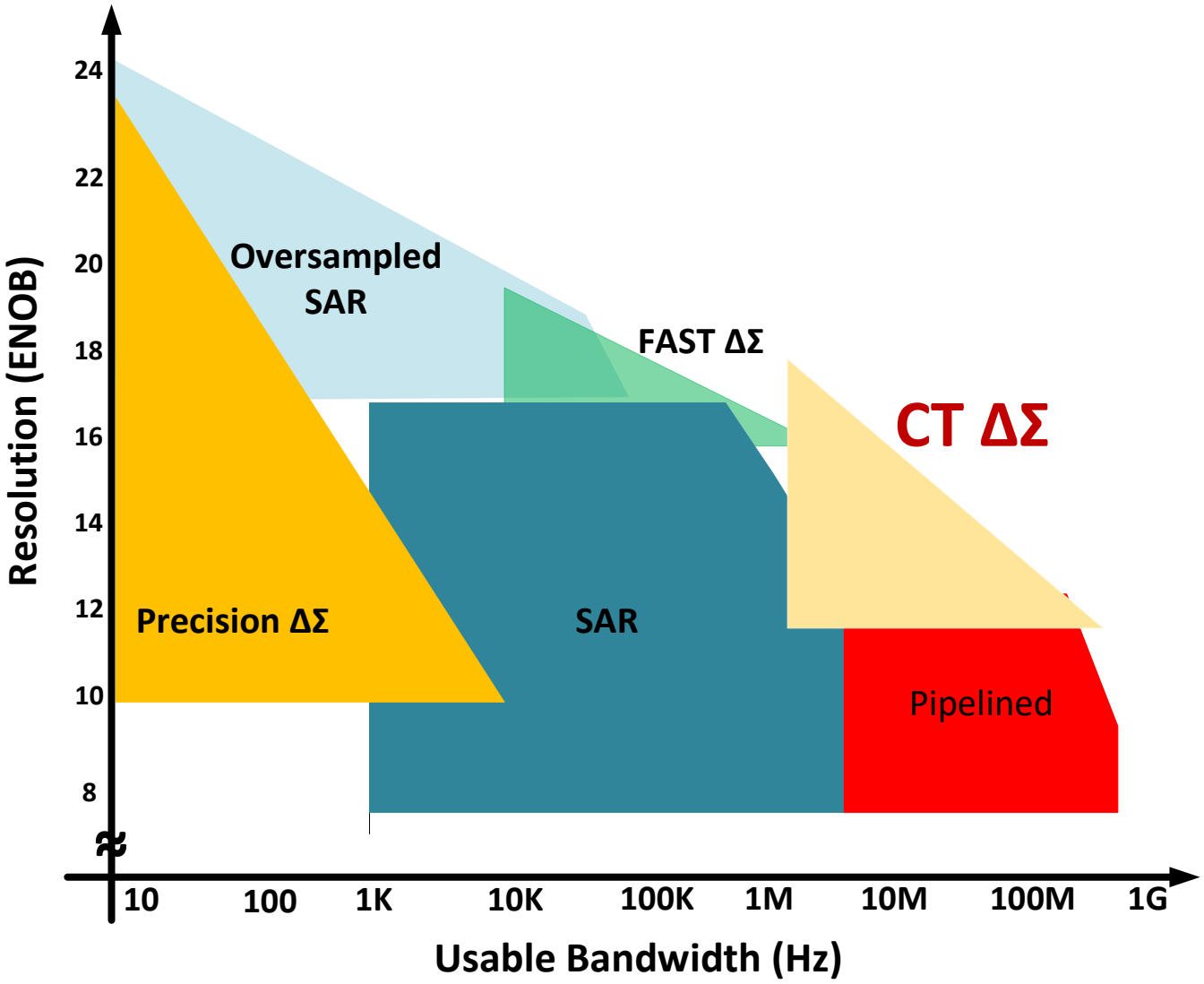
ADC Types

– Several types ADC covering the spectrum



ADC Types

– Several types ADC covering the spectrum

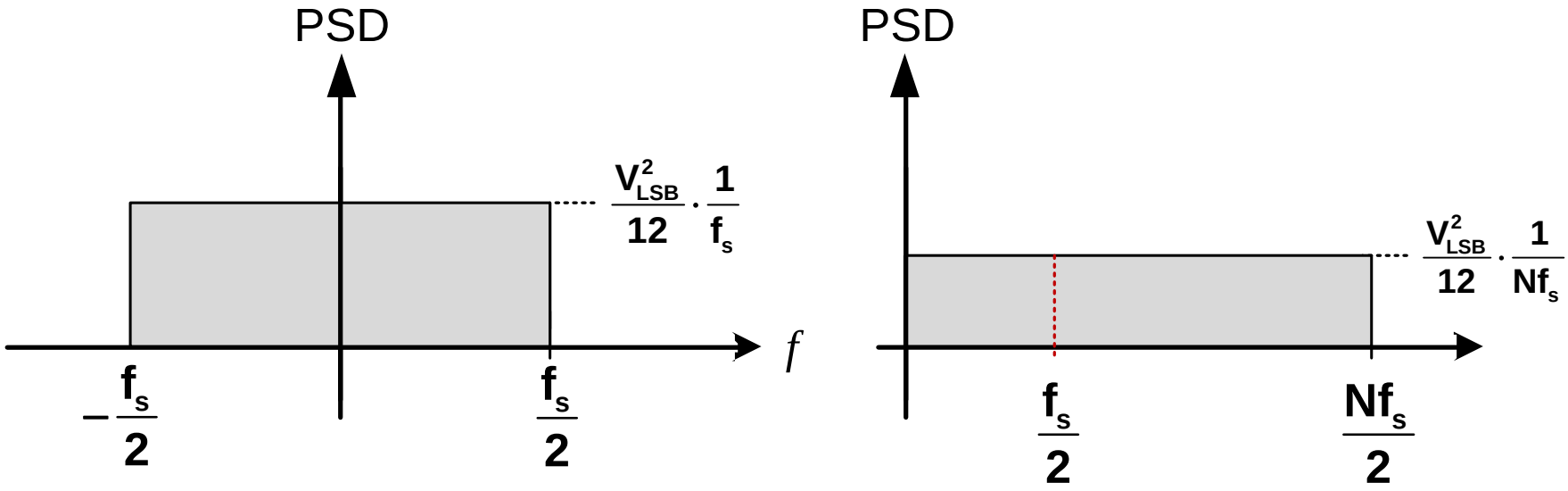


Alternative Approach: Oversampling

- **Improving SNR for a band-limited signal**
  - **Increasing # of quantization levels → smaller V_{LSB}**

$$\overline{q_E^2} = \frac{V_{LSB}^{\ 2}}{12}$$

  - **Increase the sampling frequency**



Oversampling

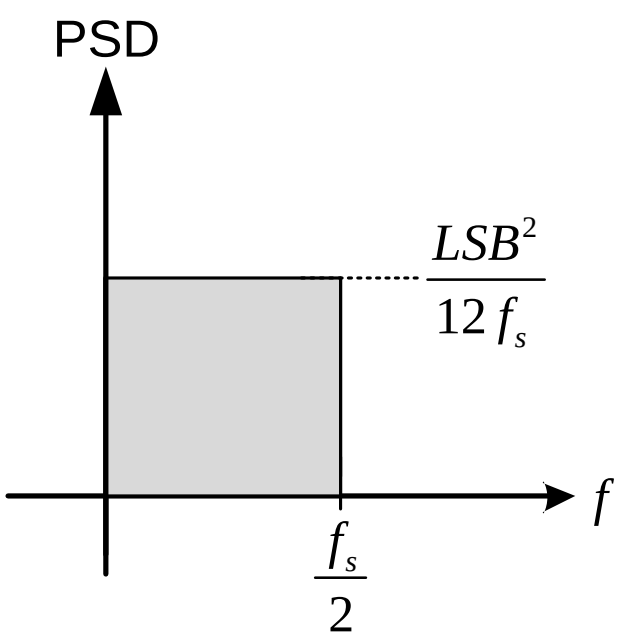
- **Doubling the oversampling ratio (OSR)**
  - **Halves the quantization *power***
  - **Increases SNR by 3dB**

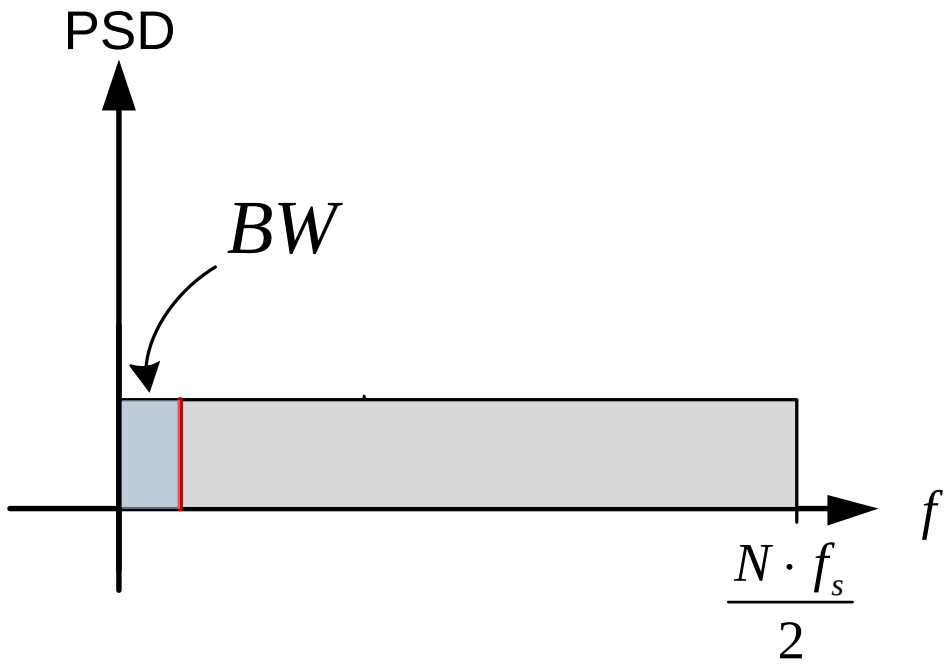
$$OSR = \frac{f_s}{2f_B}$$

- **4-bit flash ADC @ 100 MHz**
  - **OSR=1 (Nyquist) SNR=25.7dB**
  - **OSR=4 SNR=31.7dB**

Noise-Shaping & Oversampling

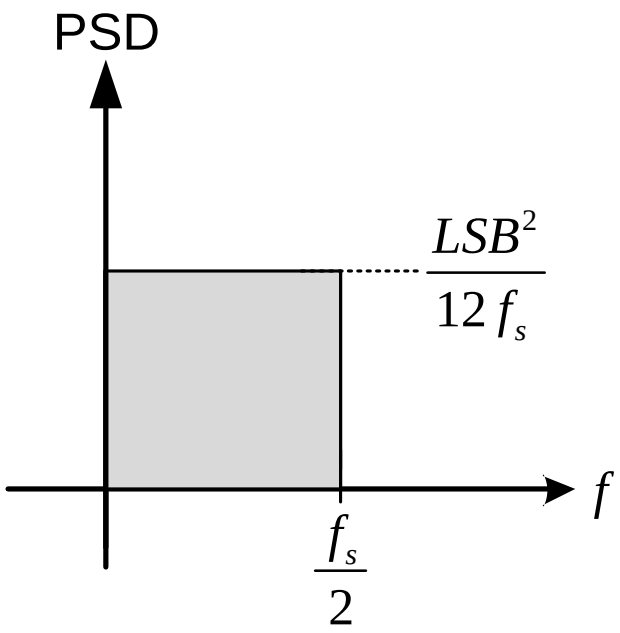
- **Using both oversampling and noise-shaping**

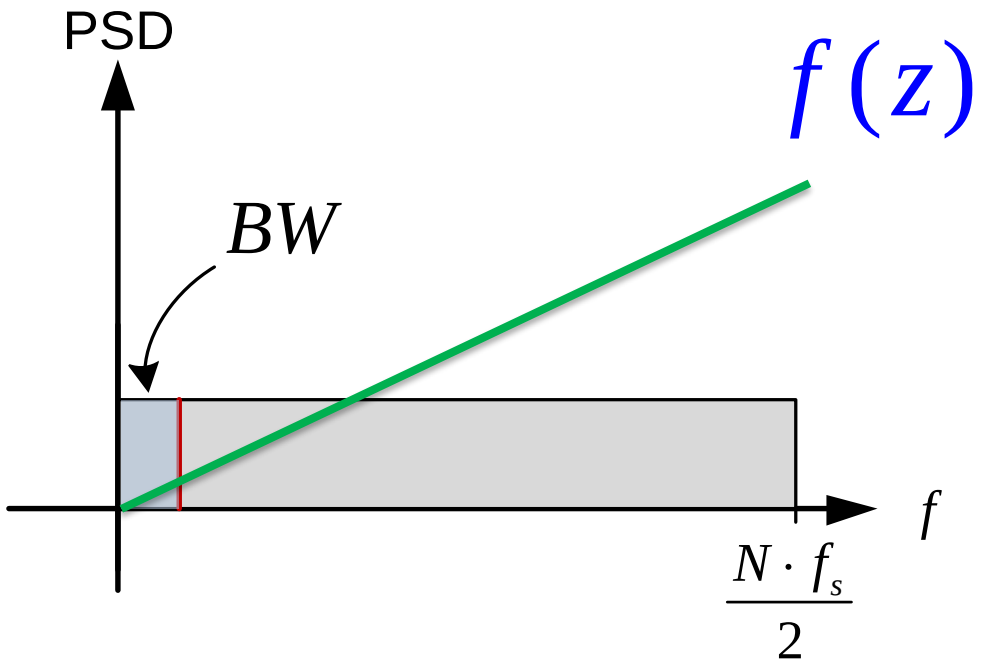




Noise-Shaping & Oversampling

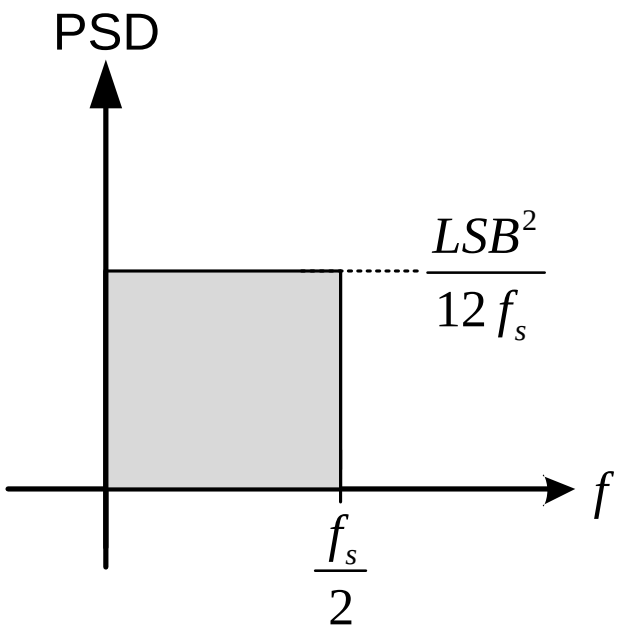
- **Using both oversampling and noise-shaping**

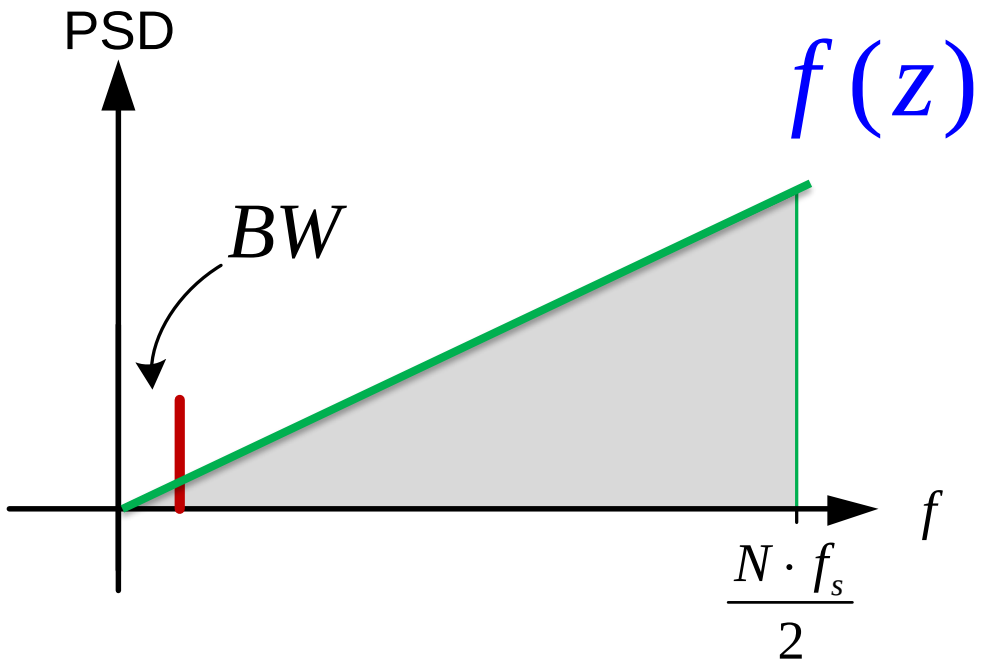




Noise-Shaping & Oversampling

- **Using both oversampling and noise-shaping**





Frequency Domain Analysis

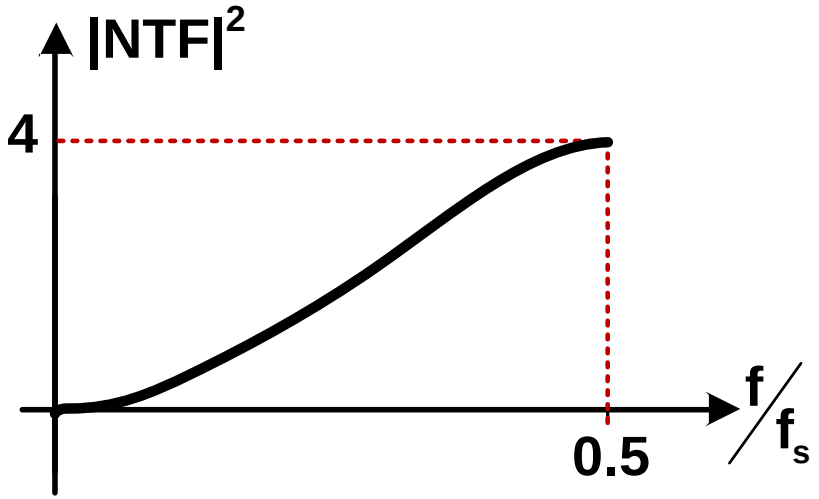
$$Y(n) = q_E(n) - q_E(n-1)$$

- **By taking the $\mathcal{Z}$-transform**

$$\Rightarrow Y(z) = (1 - z^{-1})q_E(z)$$

$(1 - z^{-1})$: *NTF*

- **The NTF above is**



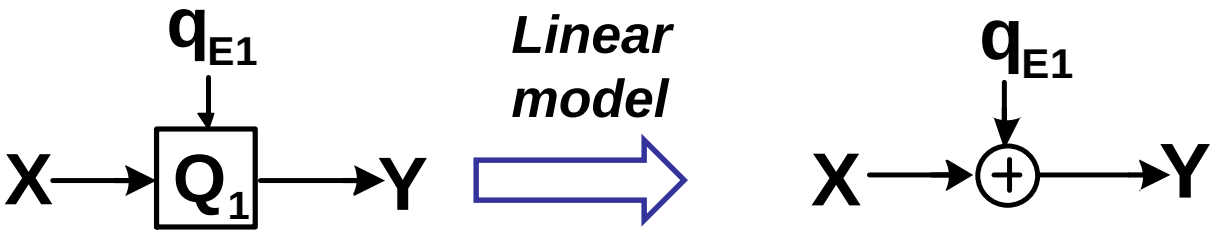
The quantization noise is shaped by the NTF filtering, and much of it is pushed to the Nyquist

Implementation

- **We are aiming to implement**

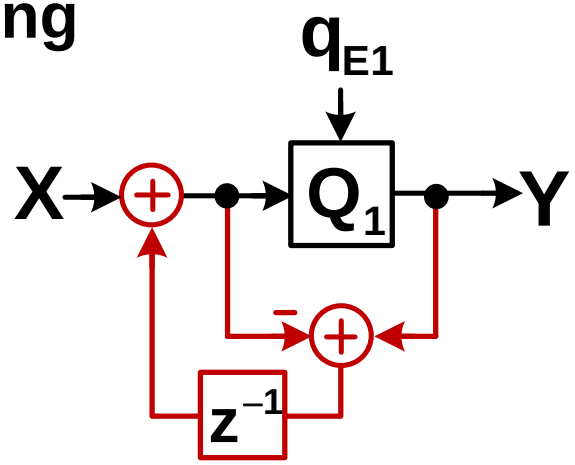
$$Y(z) = (1 - z^{-1})q_E(z)$$

  - **For a Nyquist quantizer**



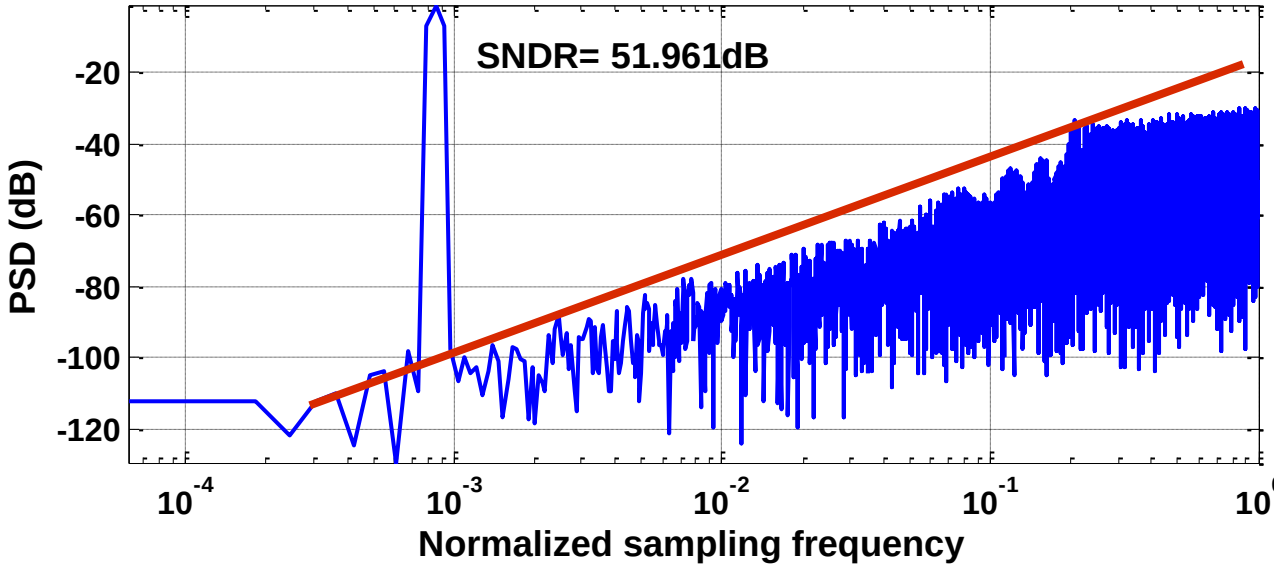
  - **For first-order noise shaping**

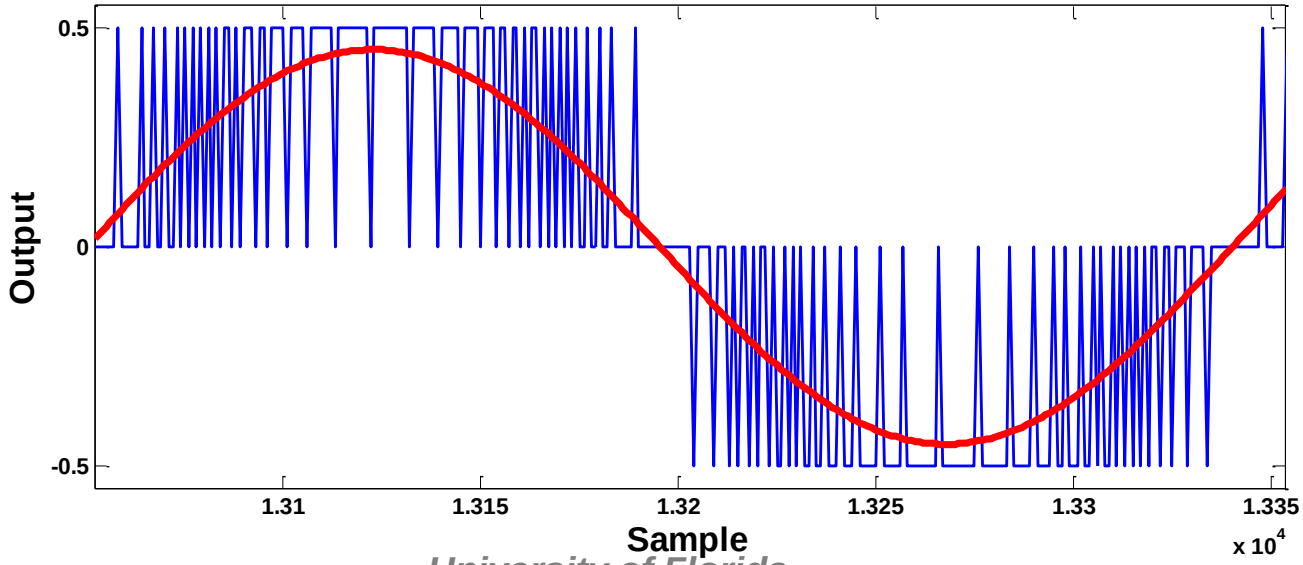
$$Y(z) = X(z) + (1 - z^{-1})q_E(z)$$



Output Spectrum

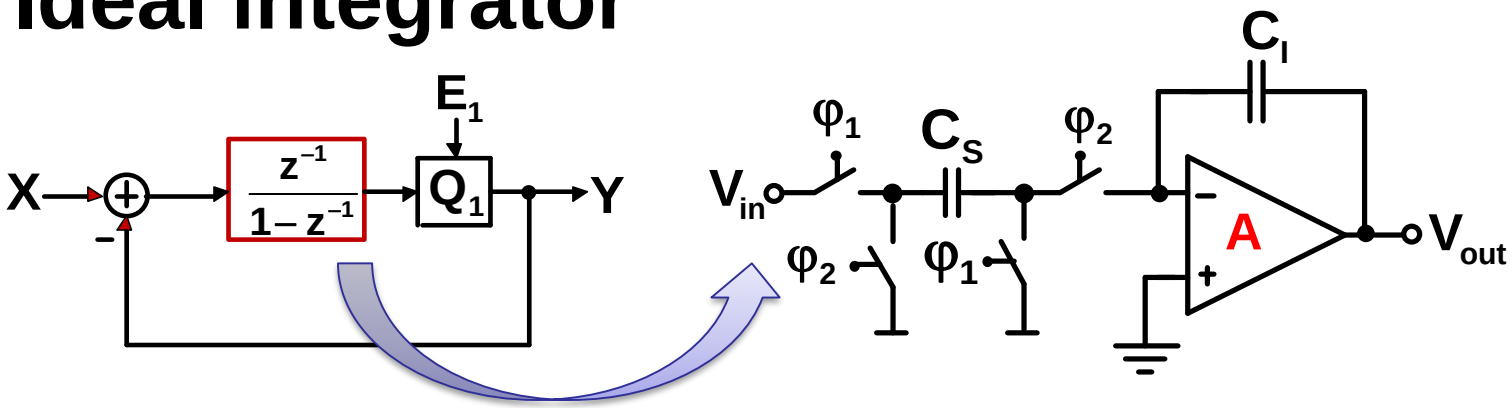
– **OSR=32, Q-levels=3**





Opamp Gain

- **Ideal integrator**



- **Limited opamp DC gain (A)**

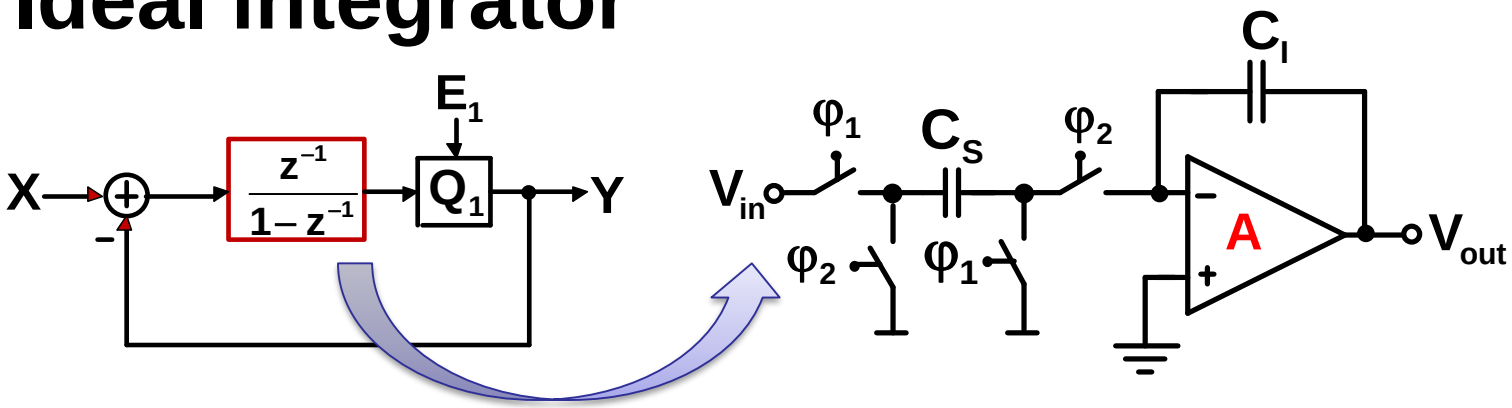
$$H(z)_{limited} = \frac{z^{-1}}{1-(1-1/A)z^{-1}}$$

- **NTF would be**

$$NTF \approx 1-(1-1/A)z^{-1}$$

Opamp Gain

- **Ideal integrator**



- **Limited opamp DC gain (A)**

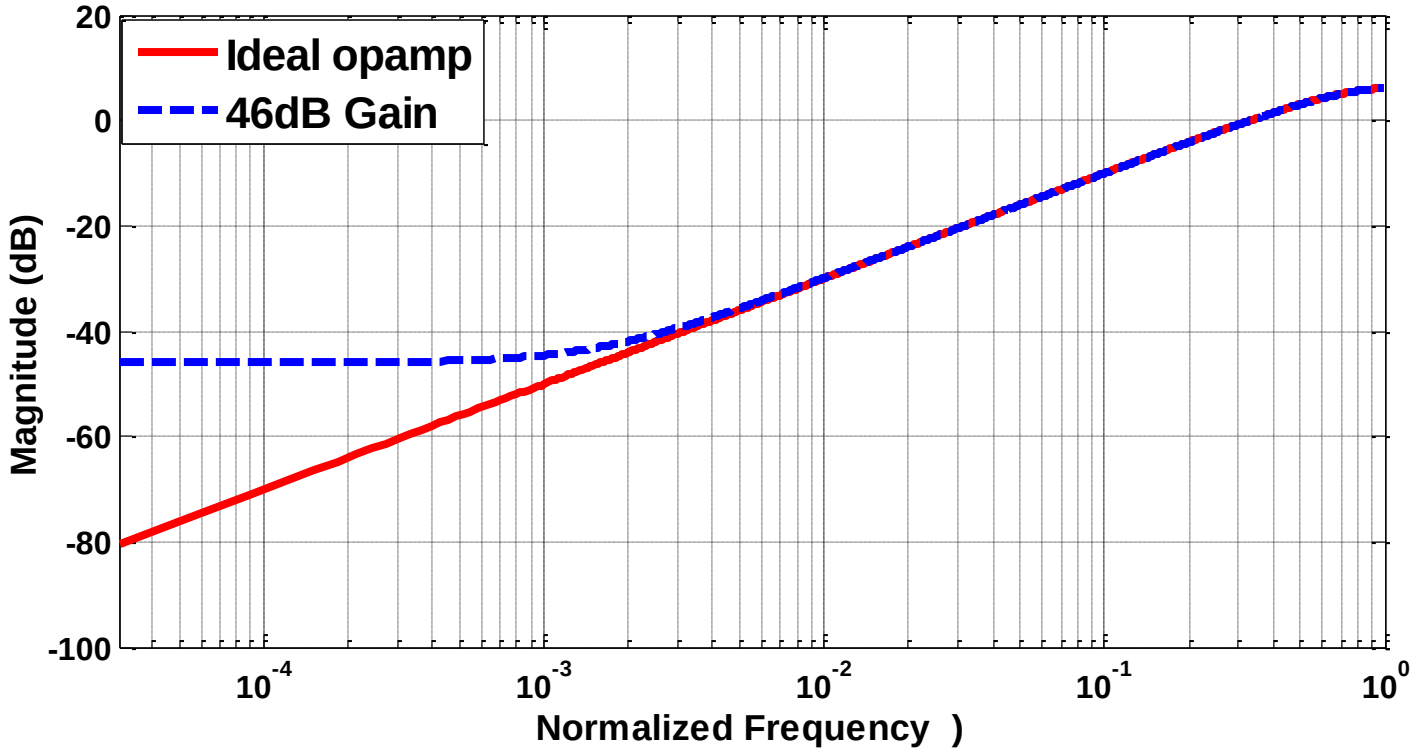
$$H(z)_{limited} = \frac{z^{-1}}{1-(1-1/A)z^{-1}}$$

- **NTF would be**

$$NTF \approx 1-(1-1/A)z^{-1} \longrightarrow \text{Zero moved by } 1/A$$

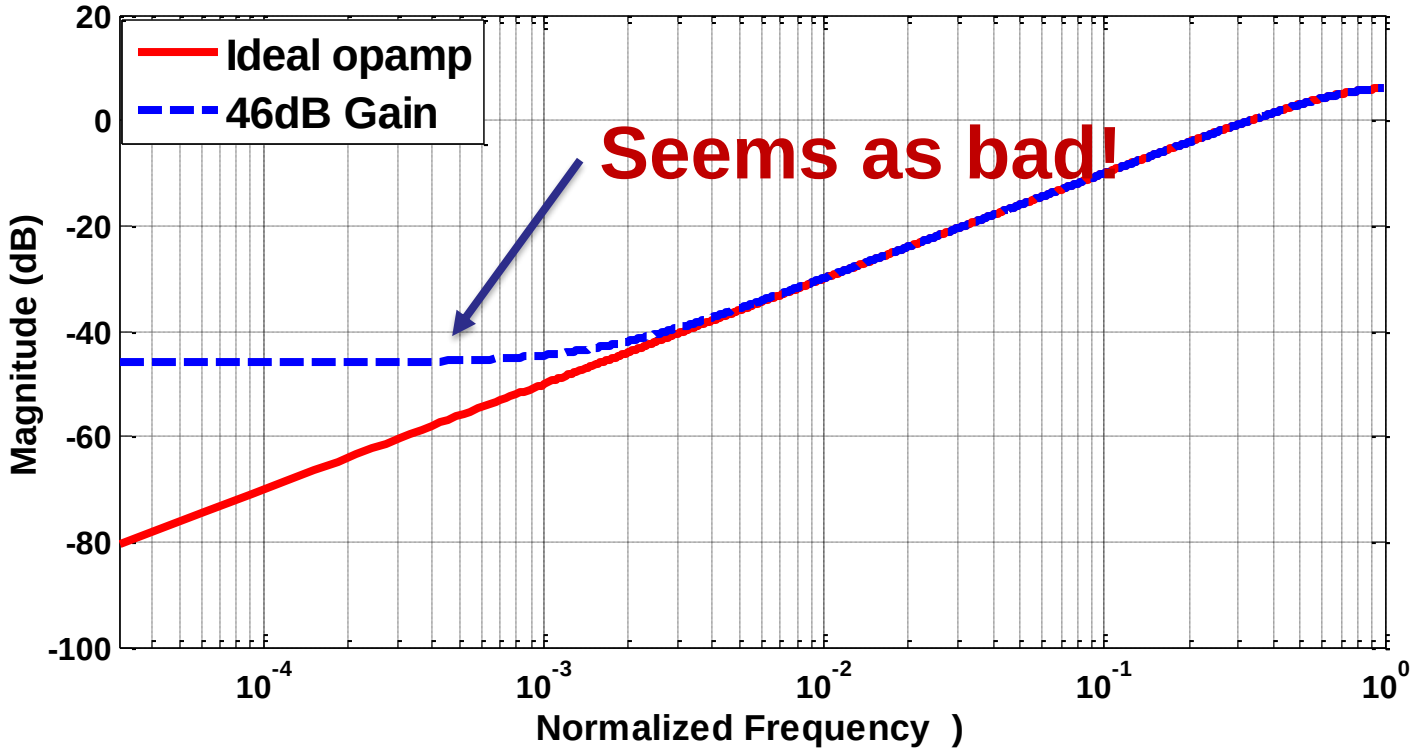
Opamp Gain

- **Depending on OSR**
  - **High OSR→ Opamp gain dominates**
  - **Low OSR → Quantization noise dominates**



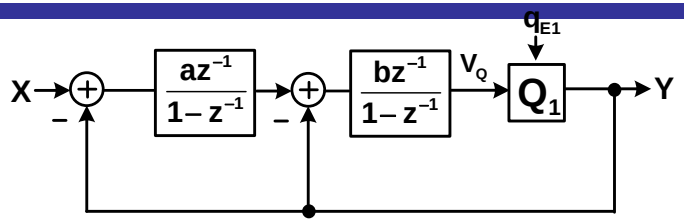
Opamp Gain

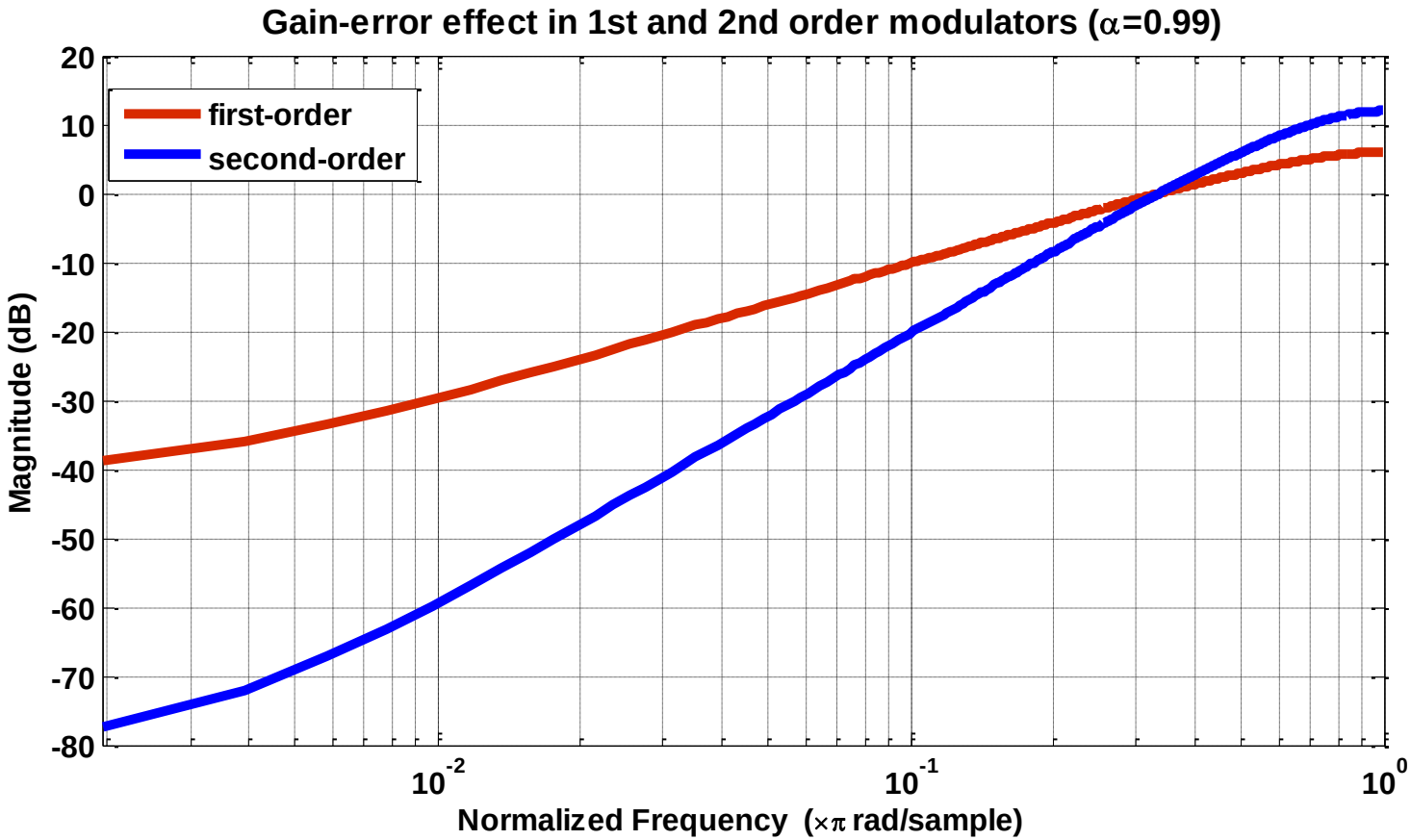
- **Depending on OSR**
  - **High OSR→ Opamp gain dominates**
  - **Low OSR → Quantization noise dominates**



Theoretical gain-error effect

– 2nd Order DSM

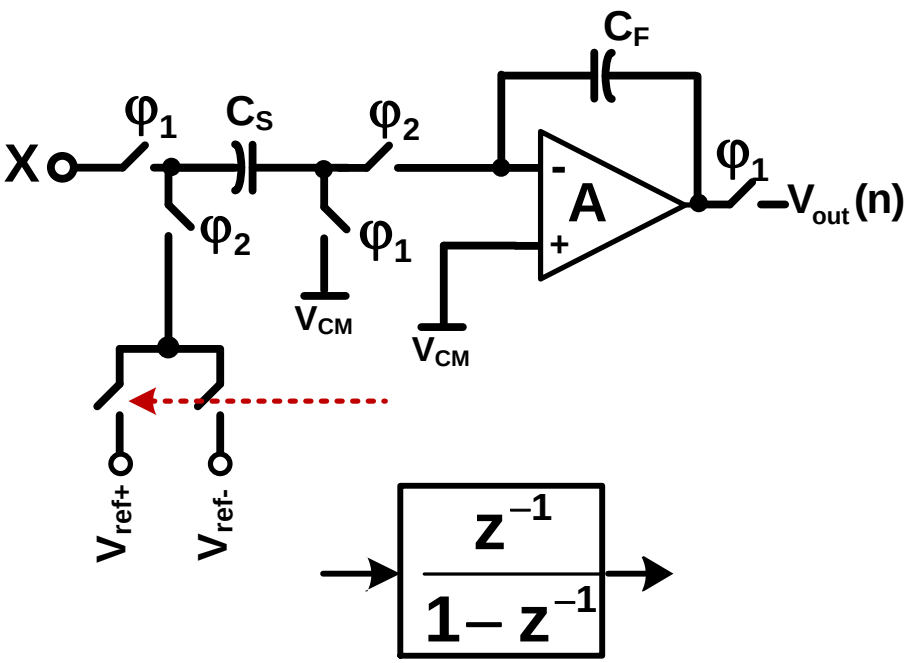


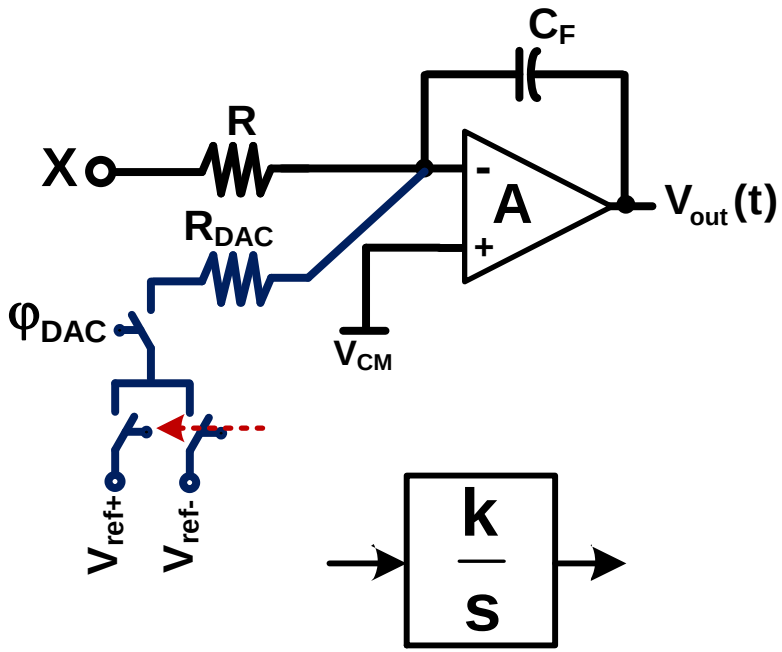


– Further improvement ***using higher order*** DSM

Continuous-Time ΔΣ

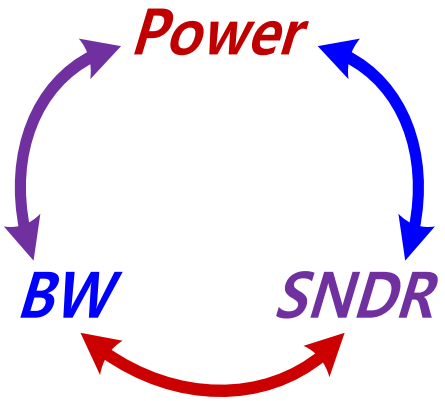
- **CT integrator Vs. DT**
  - No sampling switch ✓
  - No sampling cap ✓
  - Better Settling and Slewing ✓
  - RC Variation ✗



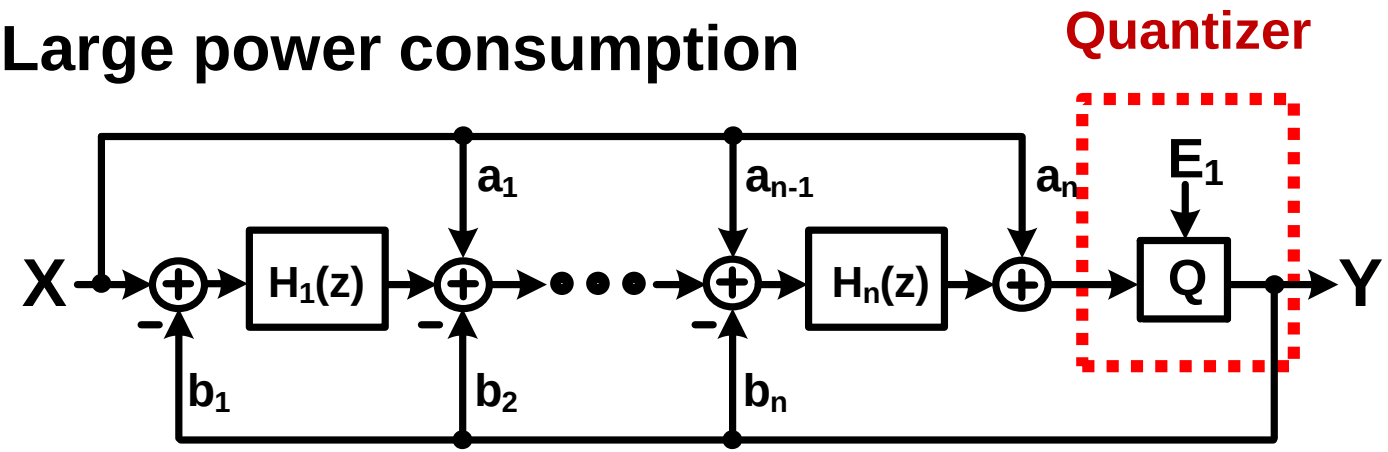


ΔΣ Modulators

- **Trade-off (Figure of Merit)**
  - High SQNR
  - High bandwidth
  - Low Power

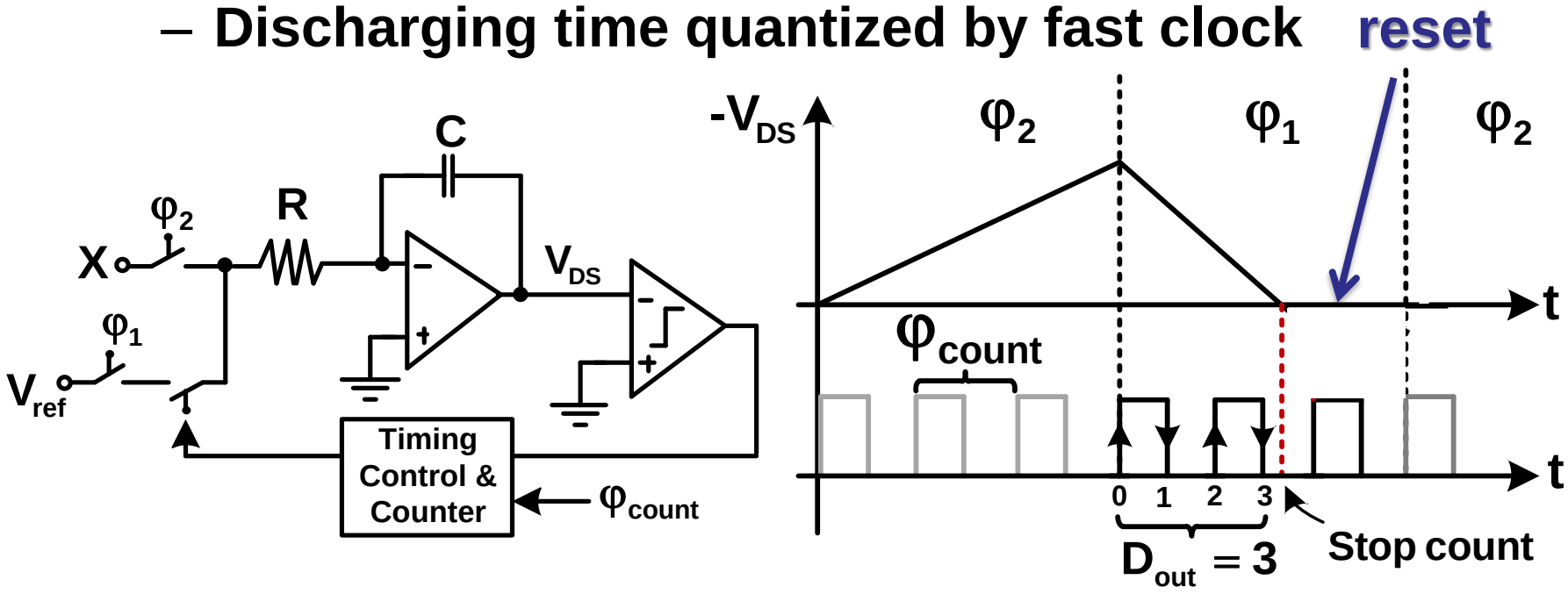


- **Back-end quantizer**
  - Typically Flash
  - Memoryless
  - Large power consumption



Traditional Dual-Slope

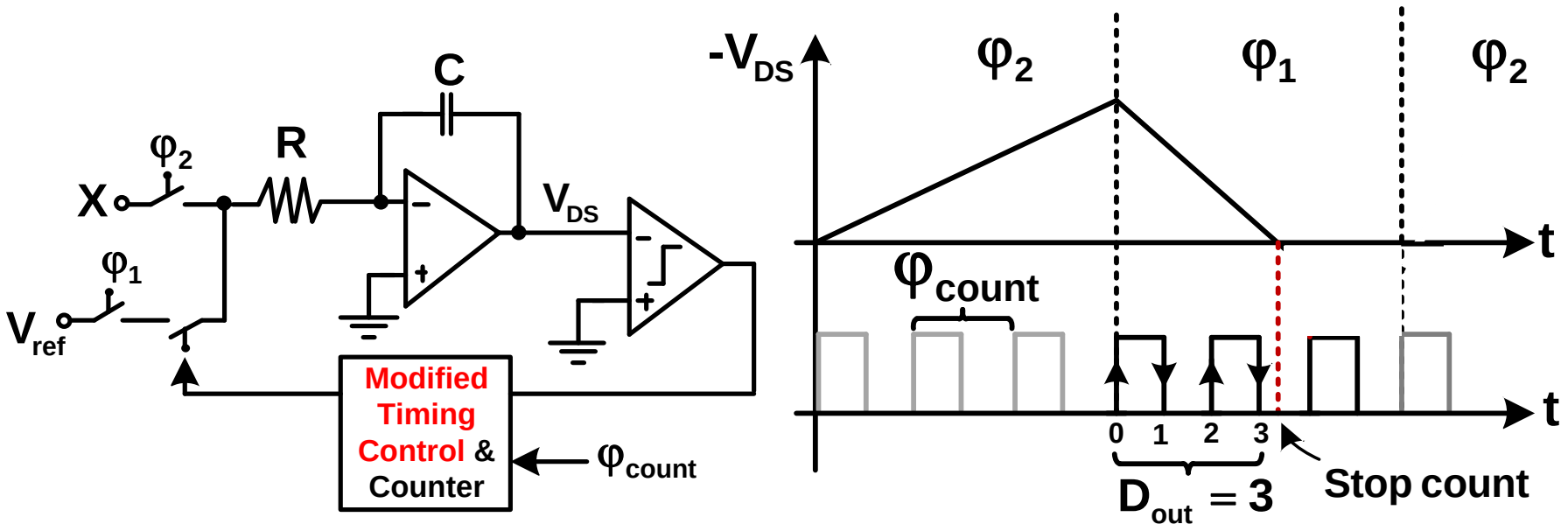
- **Simple ADC using time as media**
  - **Signal is sampled in one phase, Discharged in the other phase**
  - **Discharging time quantized by fast clock**



$$D_{out}(n) = X(n) + q_e(n)$$

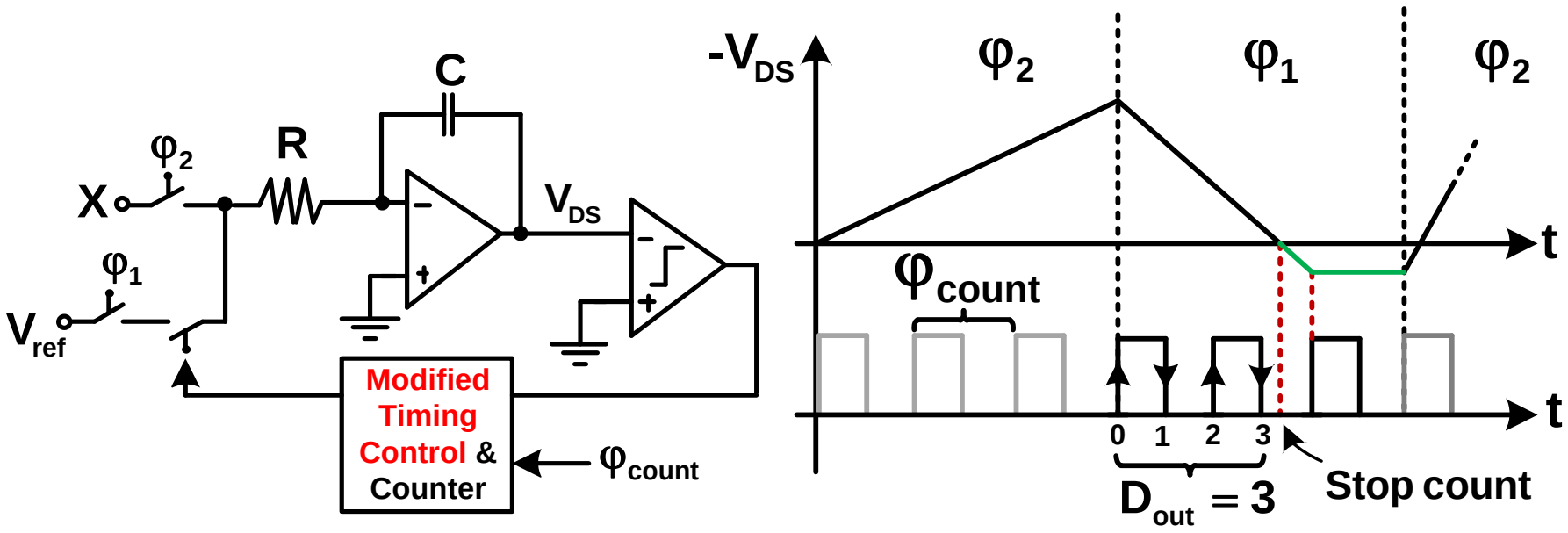
Noise-Shaped Integr. Quant.

- **Small modification**
  - Input is sampled in the same fashion
  - Discharging until the next edge *after* zero crossing



Noise-Shaped Integr. Quant.

- **Small modification**
  - Input is sampled in the same fashion
  - Discharging until the next edge *after* zero crossing

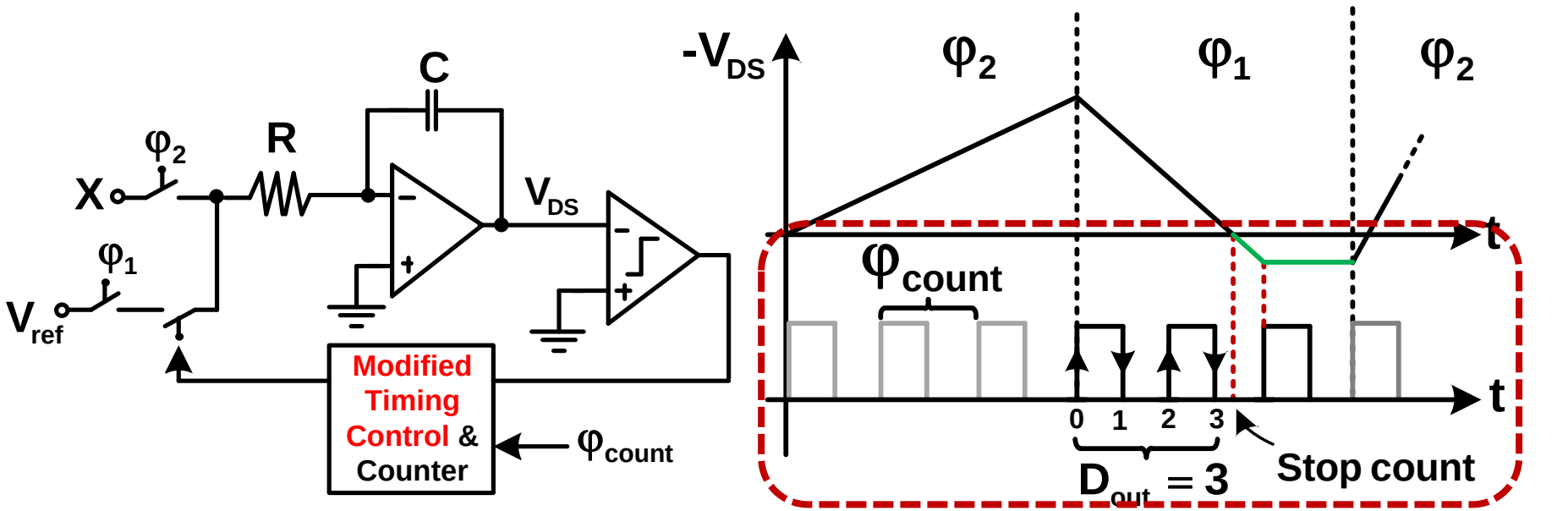


$$D_{out}(n) = X(n) - q_e(n-1) + q_e(n)$$

$$D_{out}(z) = X(z) + (1 - z^{-1}) \cdot q_e(z)$$

Noise-Shaped Integr. Quant.

- **Small modification**
  - Input is sampled in the same fashion
  - Discharging until the next edge *after* zero crossing

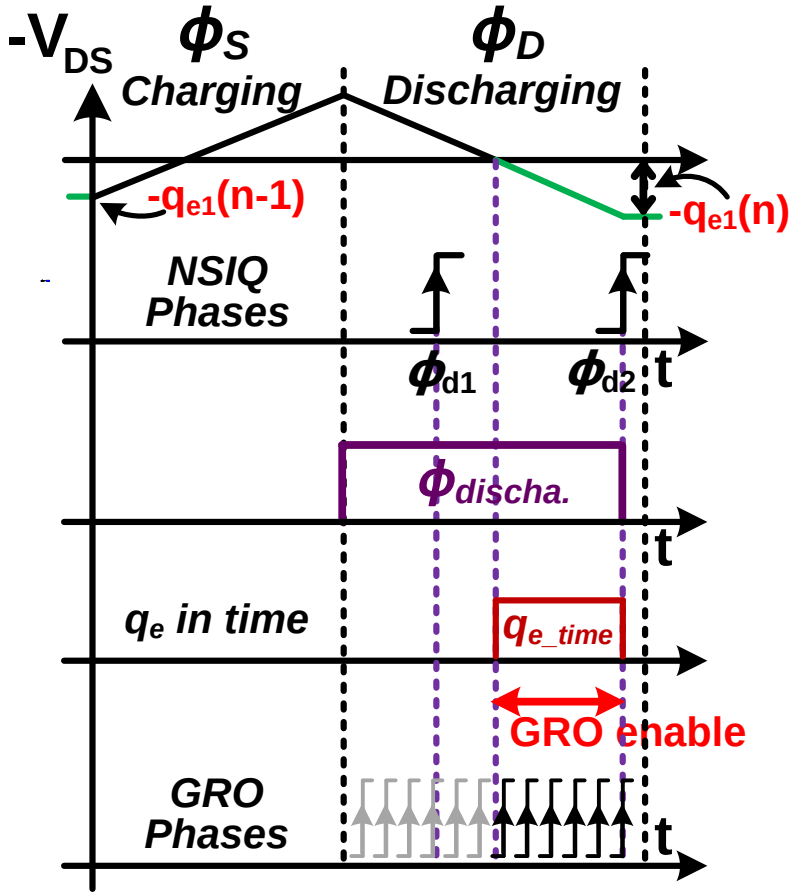


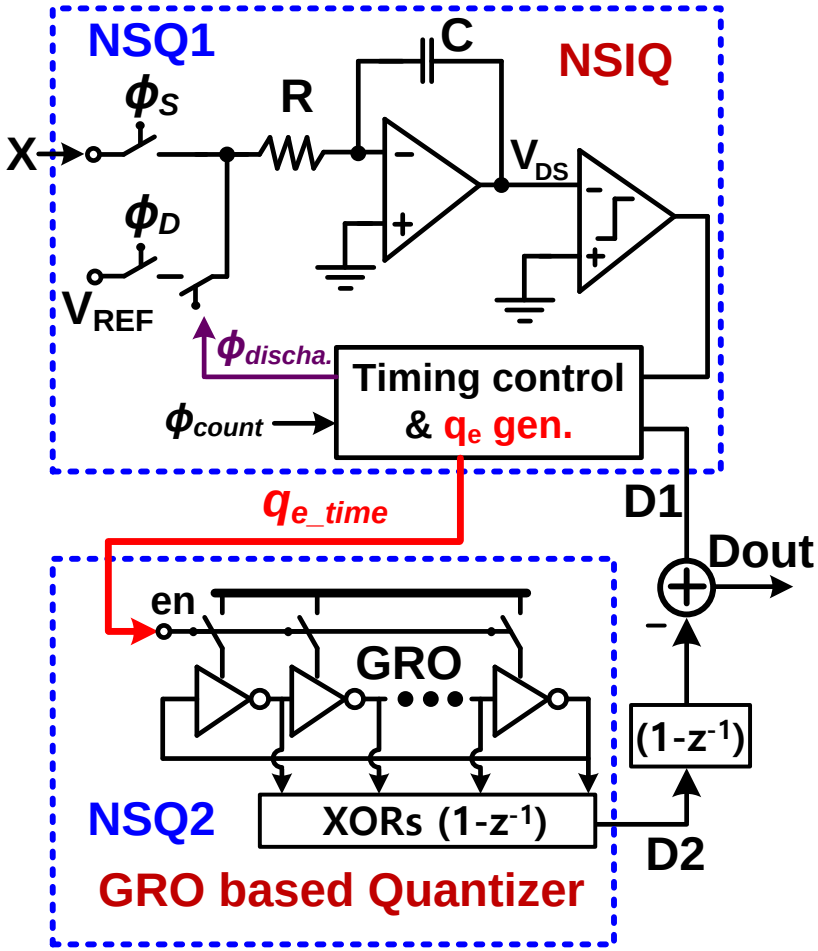
$$D_{out}(n) = X(n) - q_e(n-1) + q_e(n)$$ Scales with CMOS

$$D_{out}(z) = X(z) + (1 - z^{-1}) \cdot q_e(z)$$

Double Noise-Shaped Quantizer

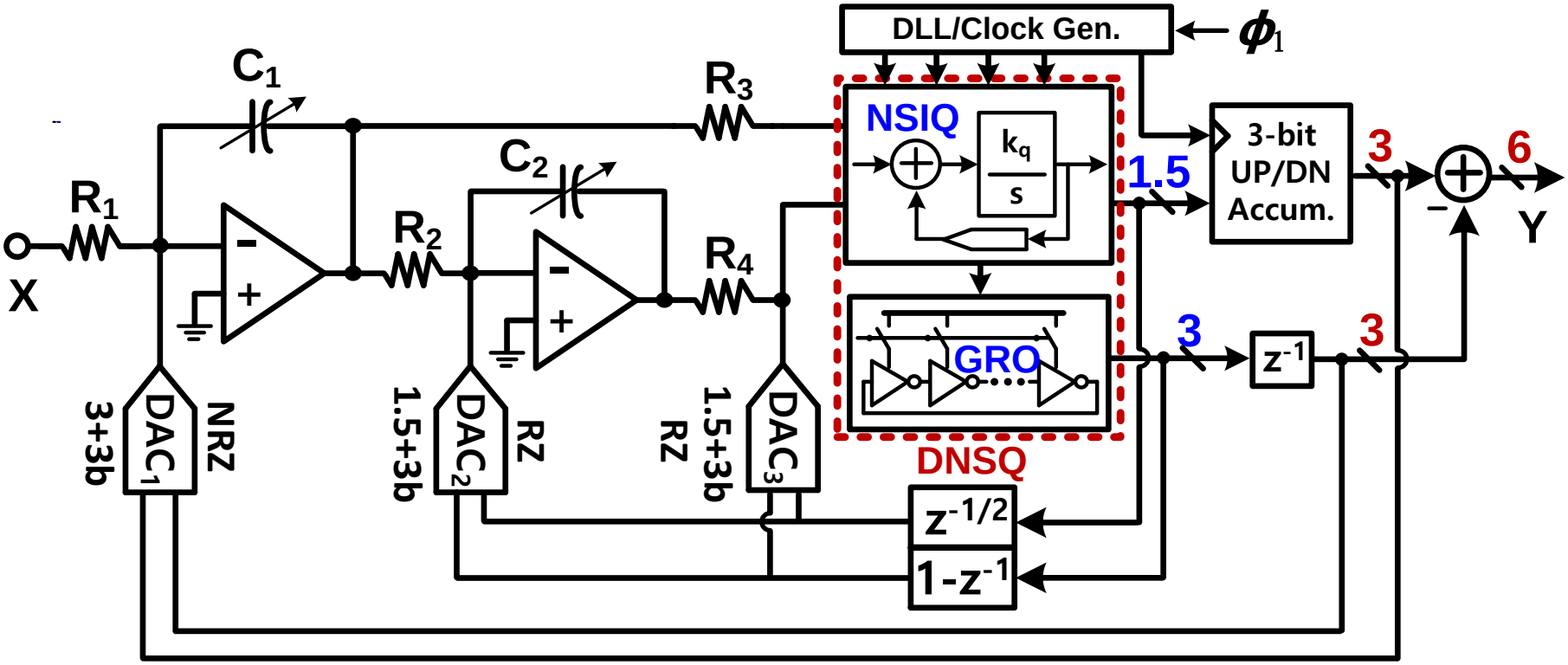
- **Double Noise-Shaped Quantizer**
  - **Working in Time/Phase domains**





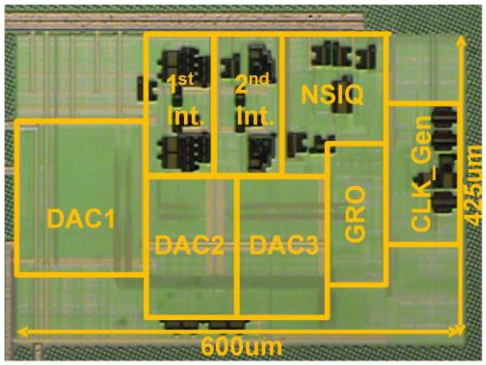
CT DSM Architecture

- **DNSQ and digital integrator at back-end**
  - **Fabricated in 130nm node**
  - **6-bit Double Noise Shaped Quantizer**

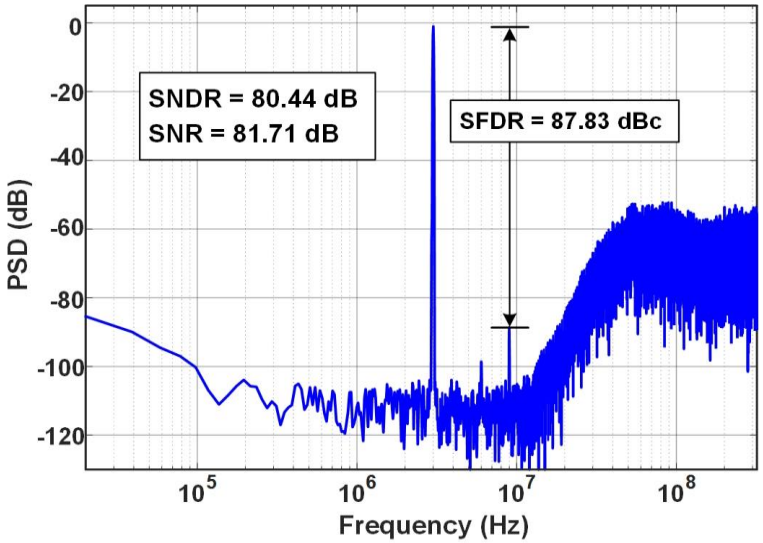


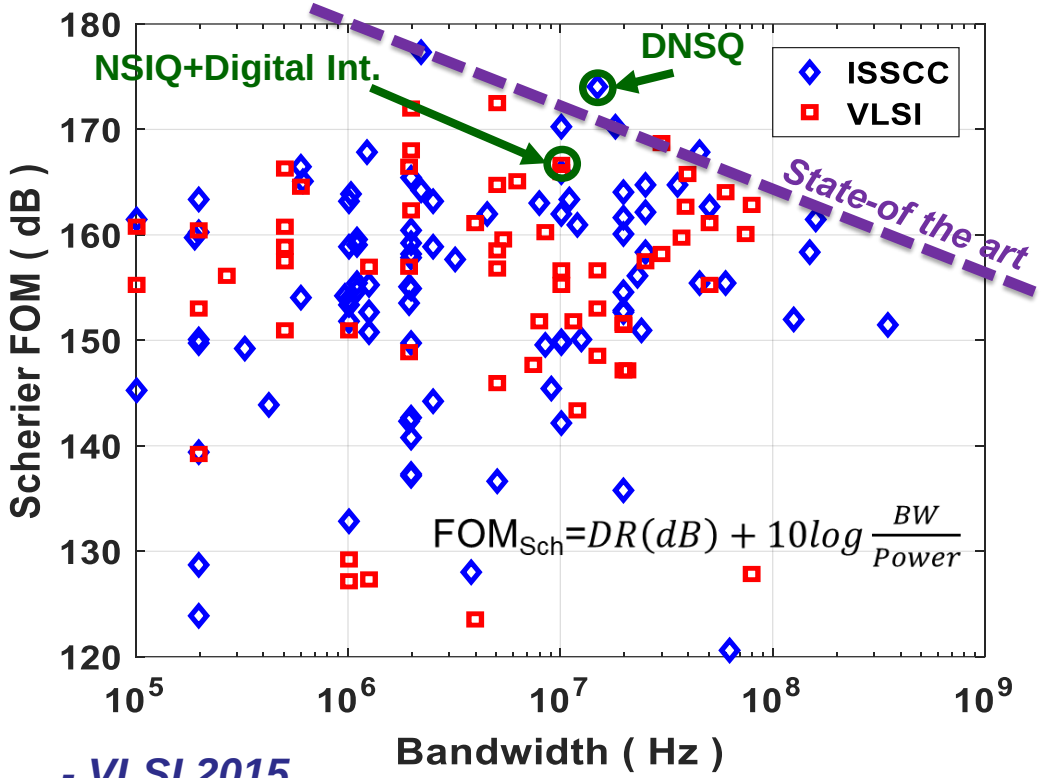
Performance Comparison

- **Measured fabricated prototype**
  - **Bested every performance down to 28nm node**



f_s = 640 MHz BW = 15 MHz





- VLSI 2015
- JSSC 2016
- ISSCC 2017
- Invited JSSC 2017 (to appear)

Sponsored by Qualcomm Inc.

Future work

- **How far we can make scale ADCs efficiently in nanometer CMOS nodes?**
- **BW limitations?**
- **Are we ready for portable 5G?**
- **…**

Currently investigating these funded by
Sponsored by Semiconductor Research Corp (SRC)
And Qualcomm Inc.

Where Were We

- **ADC pioneers**
  - **11-bit 50ks/S SAR ADC**

- 19" × 15" × 26"
- 150 lbs
- $8,500.00

Courtesy,
Analogic Corporation
8 Centennial Drive
Peabody, MA 01960

http://www.analogic.com

$$FOM = \frac{P}{2 \cdot BW \cdot 2^{ENOB}} \quad J/Conv.Step$$

  - **FoM= 2.88µJ/ Conv. Step**

Where We Are

- **Latest ADCs in same performance range with 2fJ/Conv. Step**

Where We Are

- **Latest ADCs in same performance range with 2fJ/Conv. Step**
  - **Improvement of 1.44 Billion times!**

Where We Are

- **Latest ADCs in same performance range with 2fJ/Conv. Step**
  - **Improvement of 1.44 Billion times!**
  - **Not to mention the size reduction (0.1mm^2)**

Where We Are

- **Latest ADCs in same performance range with 2fJ/Conv. Step**
  - **Improvement of 1.44 Billion times!**
  - **Not to mention the size reduction (0.1mm^2)**
- **If vehicles followed the same**

Where We Are

- **Latest ADCs in same performance range with 2fJ/Conv. Step**
  - **Improvement of 1.44 Billion times!**
  - **Not to mention the size reduction (0.1mm^2)**
- **If vehicles followed the same**
  - **In 1960s, the average MPG was about 8**

Where We Are

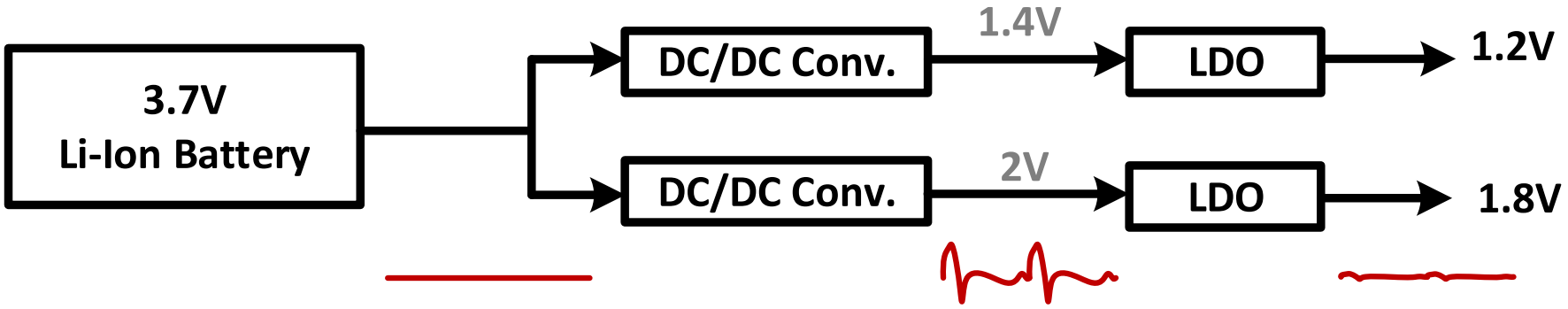
- **Latest ADCs in same performance range with 2fJ/Conv. Step**
  - **Improvement of 1.44 Billion times!**
  - **Not to mention the size reduction (0.1mm^2)**
- **If vehicles followed the same**
  - **In 1960s, the average MPG was about 8**
- **Improvement with factor of 1.44Billion means**

Where We Are

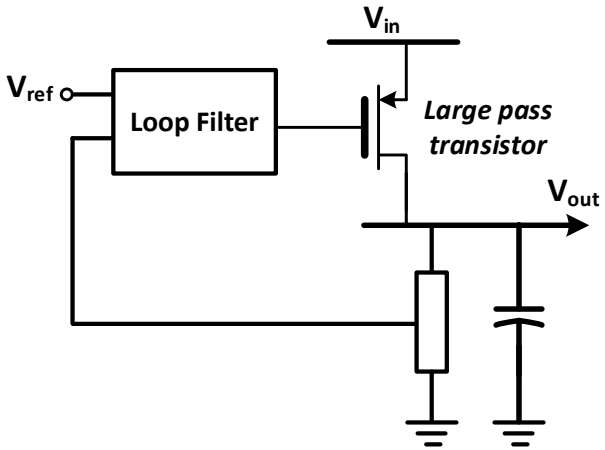
- **Latest ADCs in same performance range with 2fJ/Conv. Step**
  - **Improvement of 1.44 Billion times!**
  - **Not to mention the size reduction (0.1mm^2)**
- **If vehicles followed the same**
  - **In 1960s, the average MPG was about 8**
- **Improvement with factor of 1.44Billion means**
  - **With one drop of fuel (0.1cc) you can drive round the earth 12 times!**

Power Management

- Generate various DC voltages



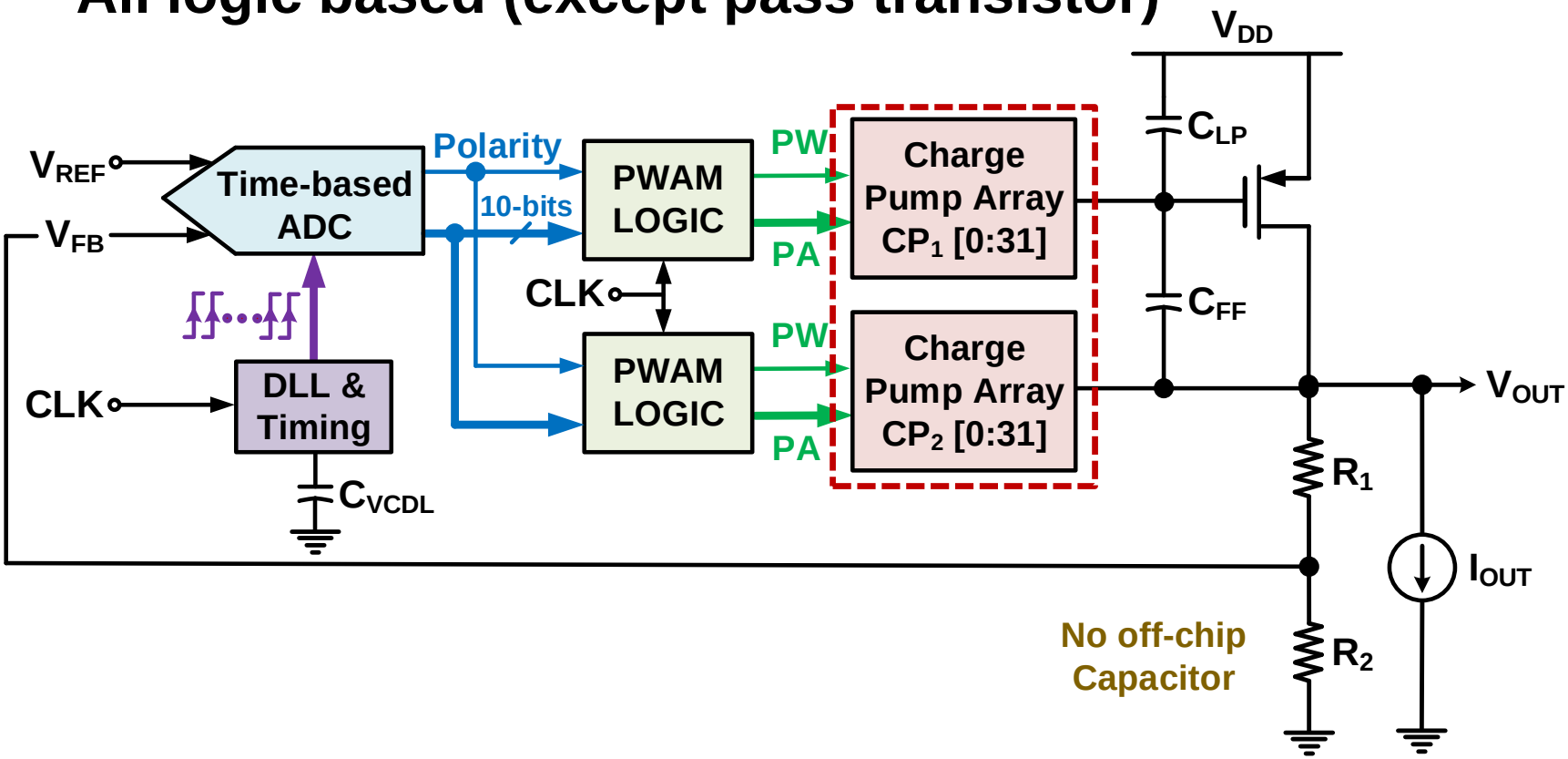
- Low-Dropout Regulators (LDO)
  - Clean voltage ripple
  - Fast transient response
  - Min. power
  - Need fast opamp



- Suffers from the same fate as ADCs

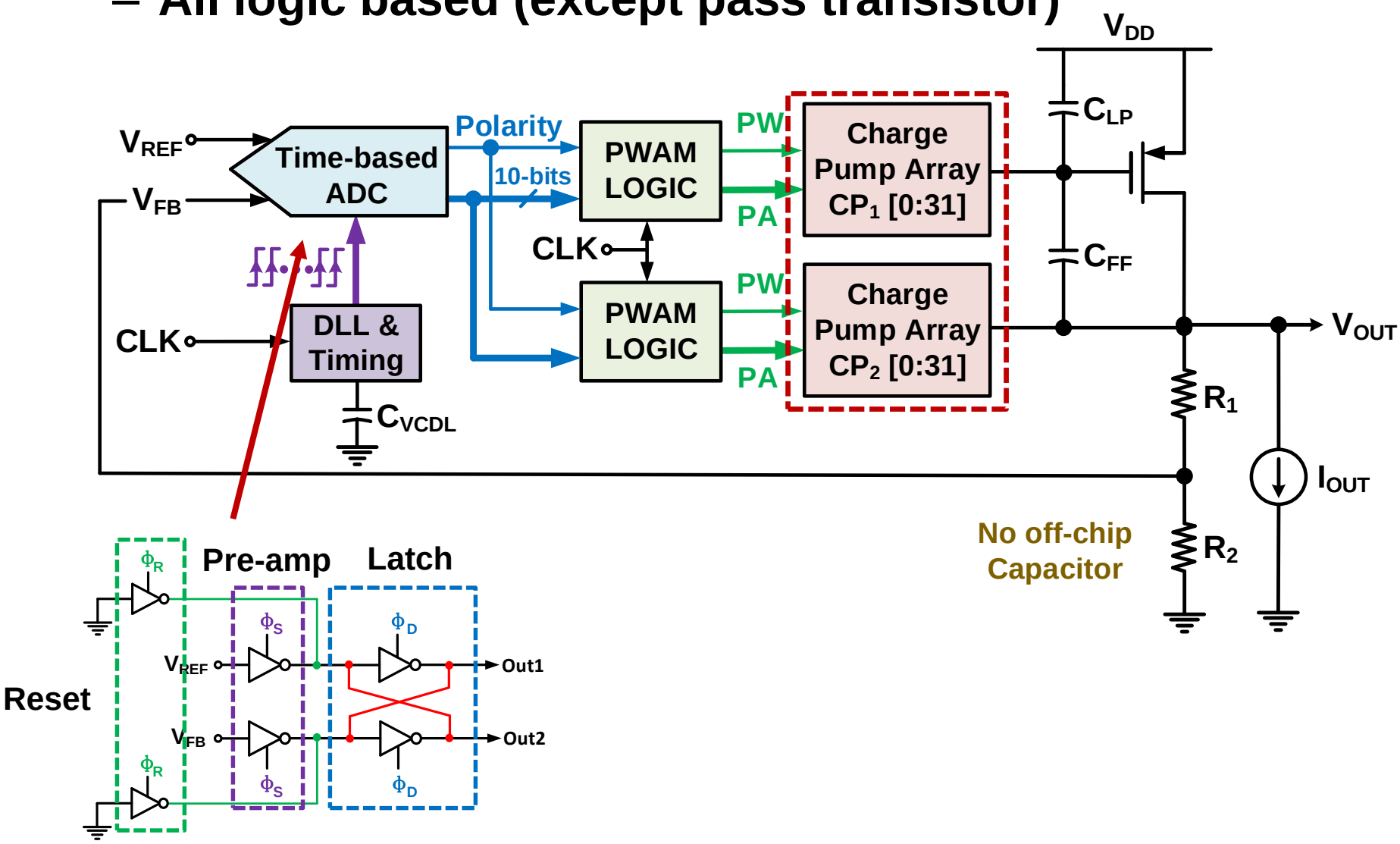
Fully Synthesizable Time-Based LDO

– All logic based (except pass transistor)



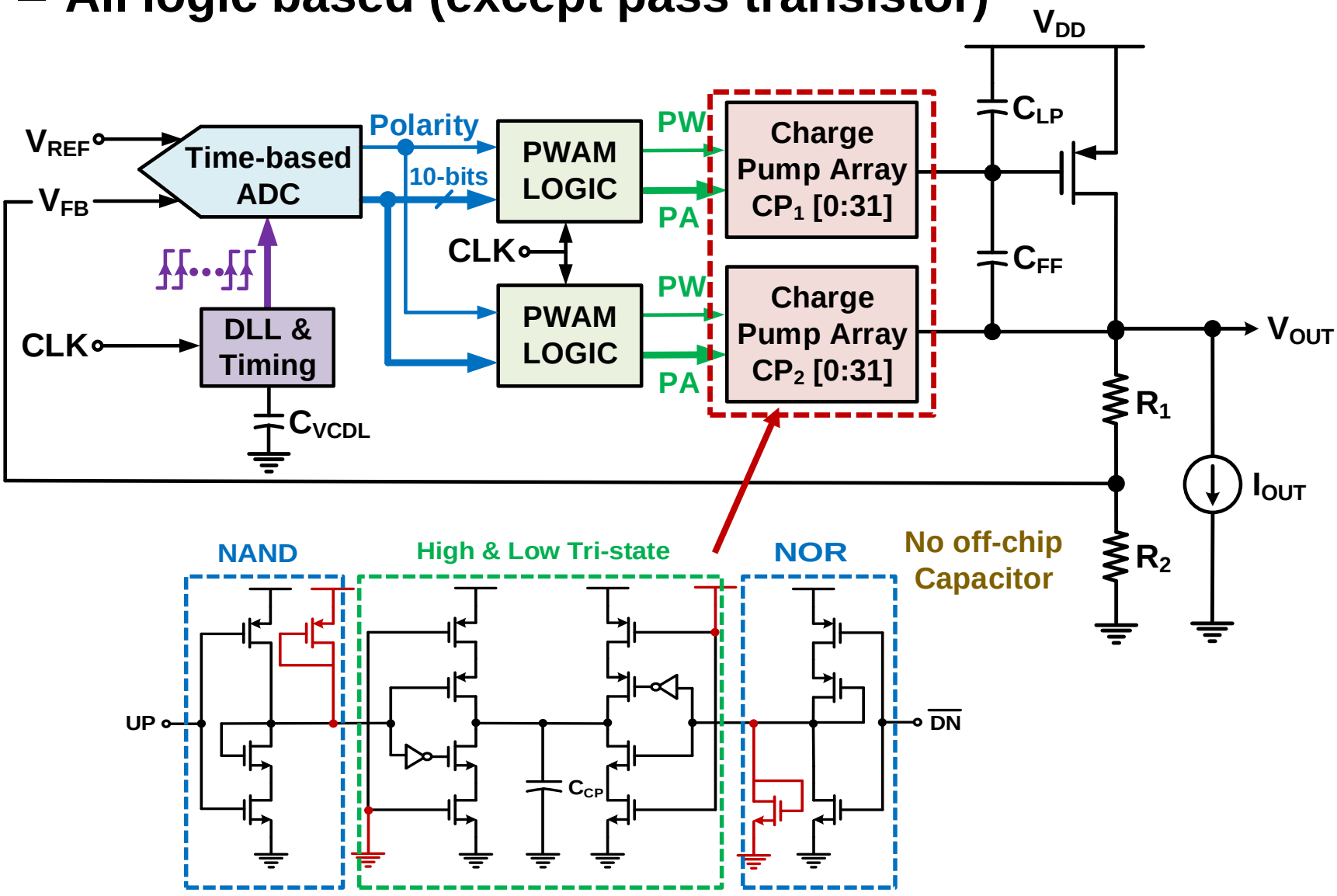
Fully Synthesizable Time-Based LDO

– All logic based (except pass transistor)



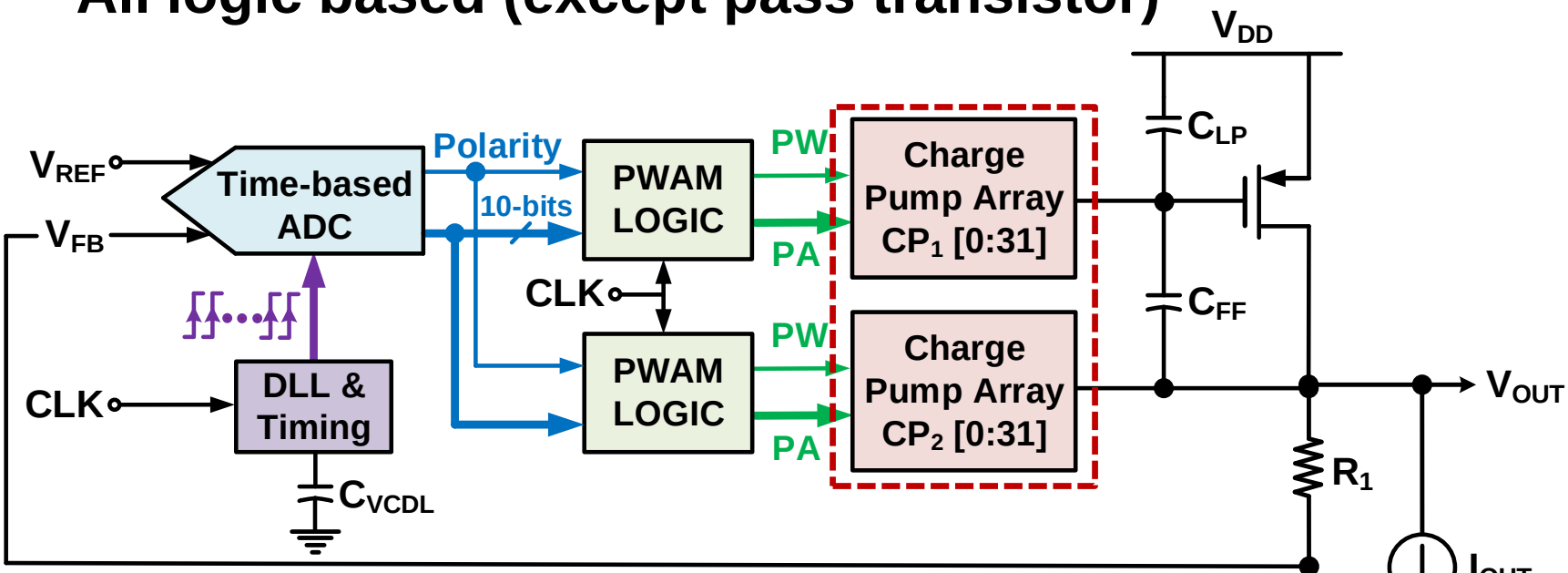
Fully Synthesizable Time-Based LDO

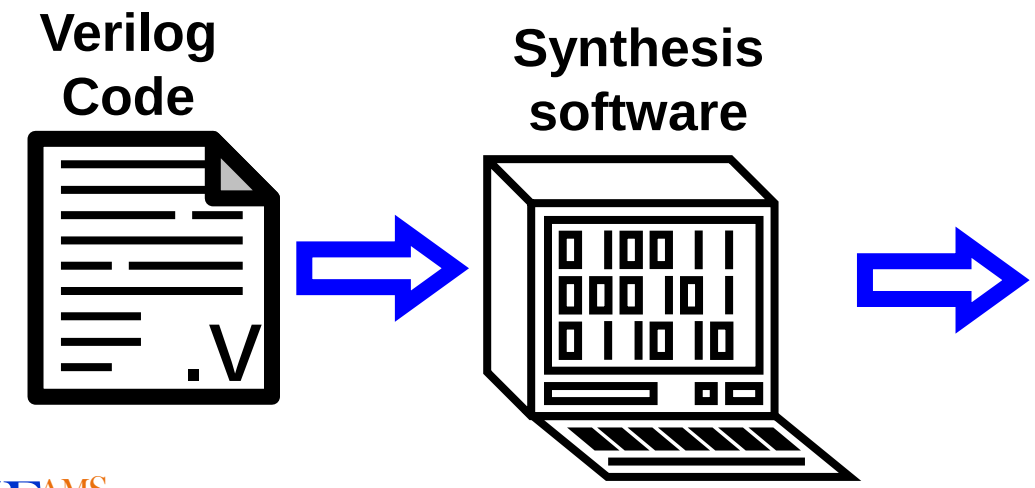
– All logic based (except pass transistor)



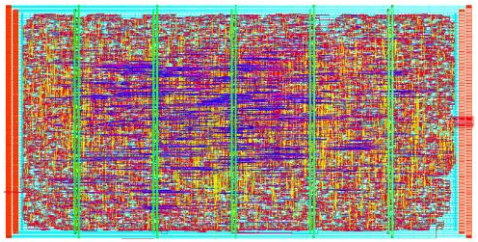
Fully Synthesizable Time-Based LDO

– All logic based (except pass transistor)





No off-chip Capacitor

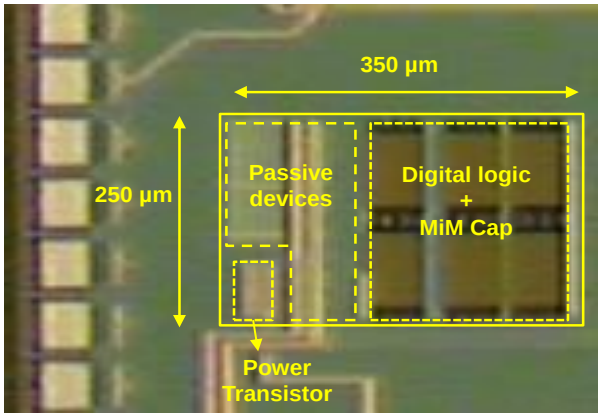


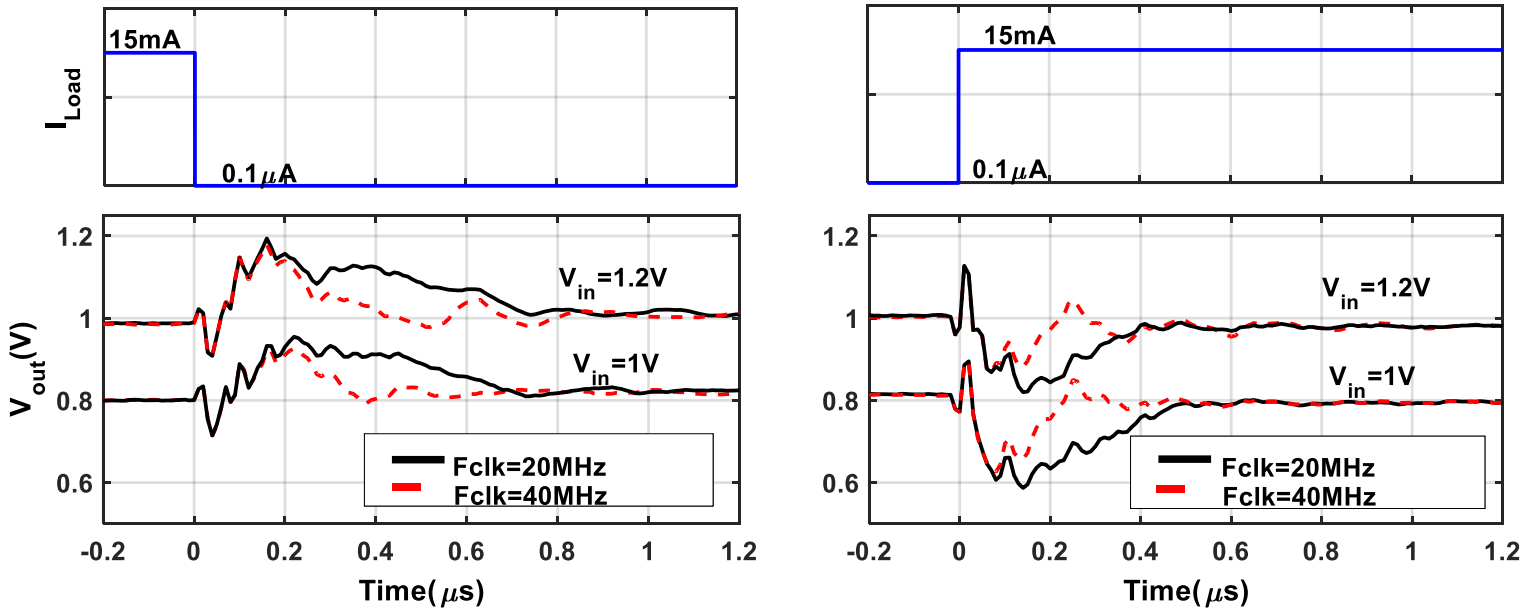
Physical Circuit

Measurement Results

- **Measured Results**
  - **0.13um process**
  - **Small Area (350X250um)**

Steady State
power consumption < 100uA





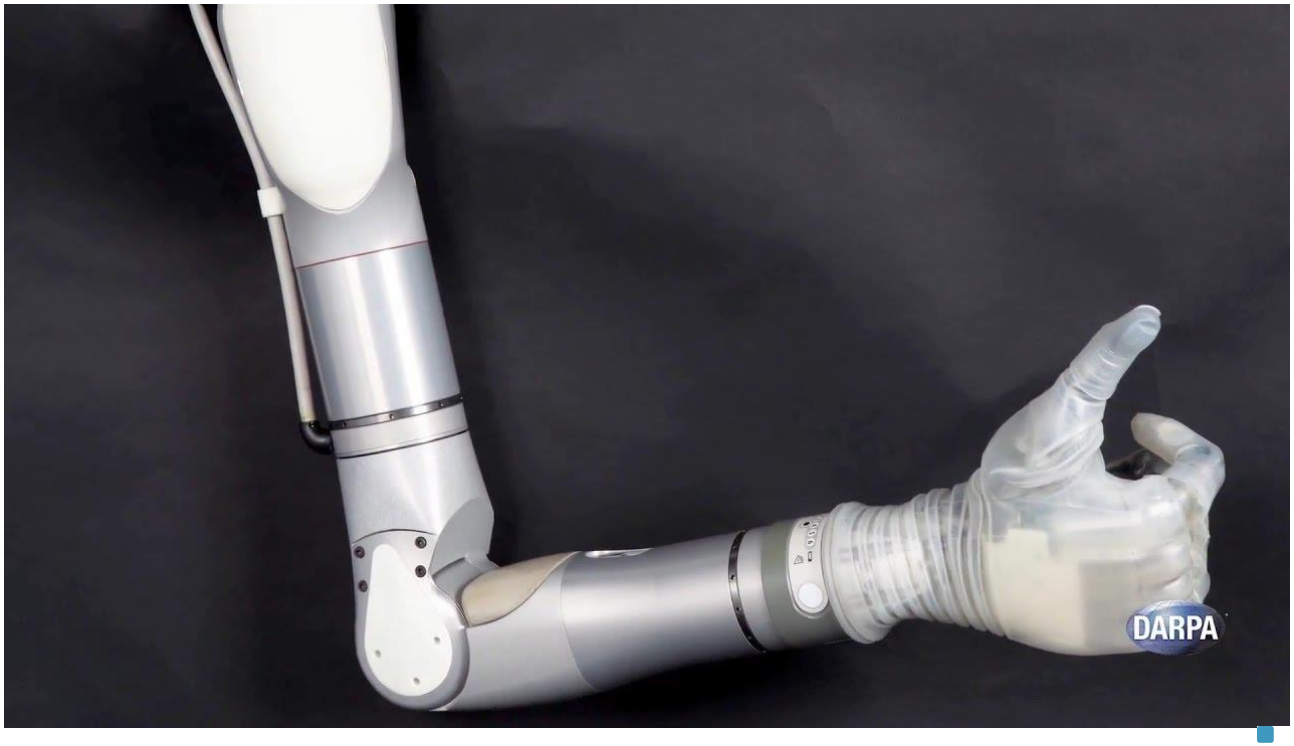
To be presented at European Solid-State Circuits (ESSCIRC)

Sponsored by Analog Devices Inc (ADI)

IMPRESS

- **Implantable Multimodal Peripheral REcording and Stimulation System**
  - **To enable bidirectional control of prosthetic limb**

DARPA LUKE arm

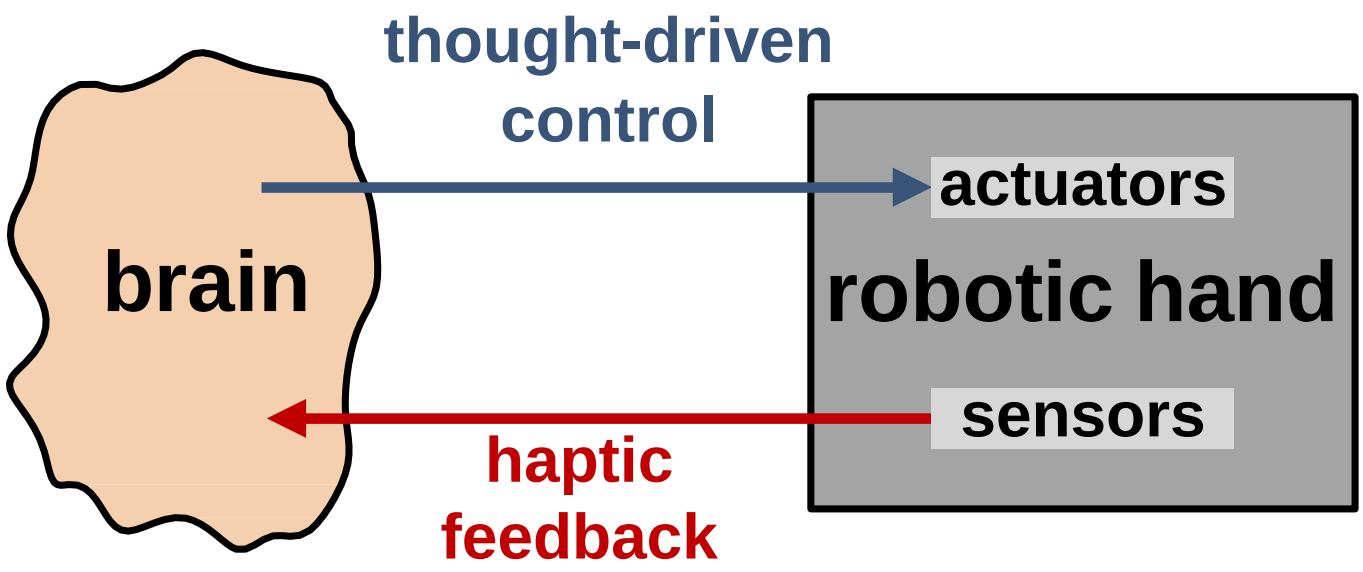


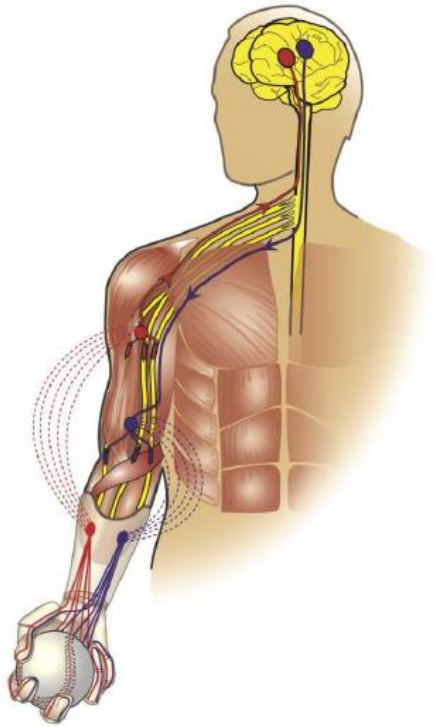
Motivation

- In collaboration with imec
- Motivation: restore
  - motor functionality
  - sensory feedback
  - temperature, pressure sensation for better control,...
  - alleviate phantom limb pain

Research Goal

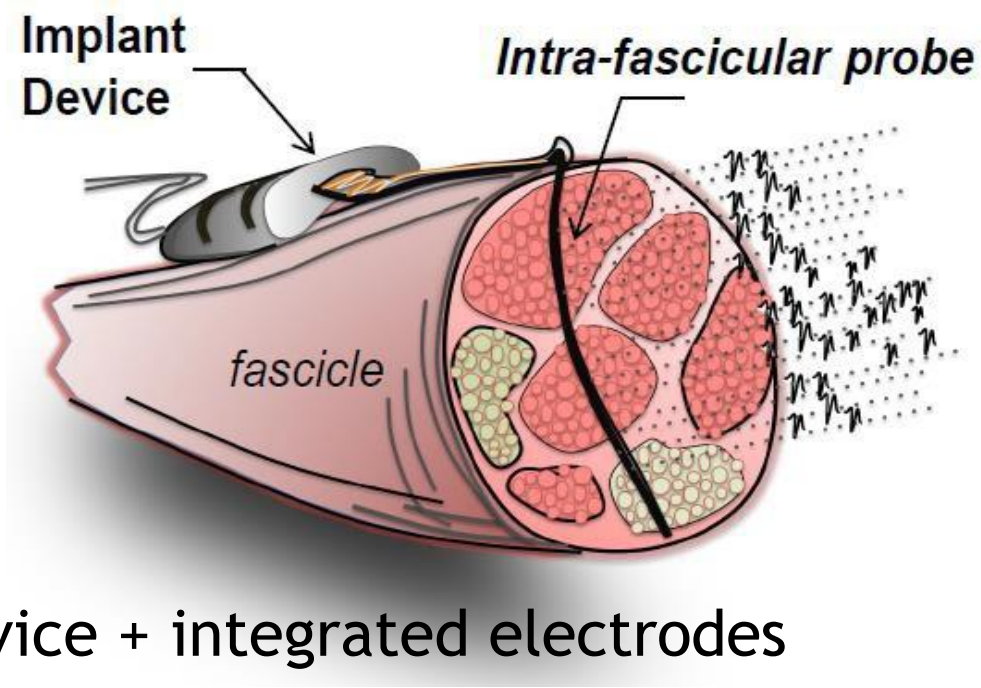
- Communication between brain of amputee and bionic arm/hand
  - Bi-directional neural interface





Proposed Solution

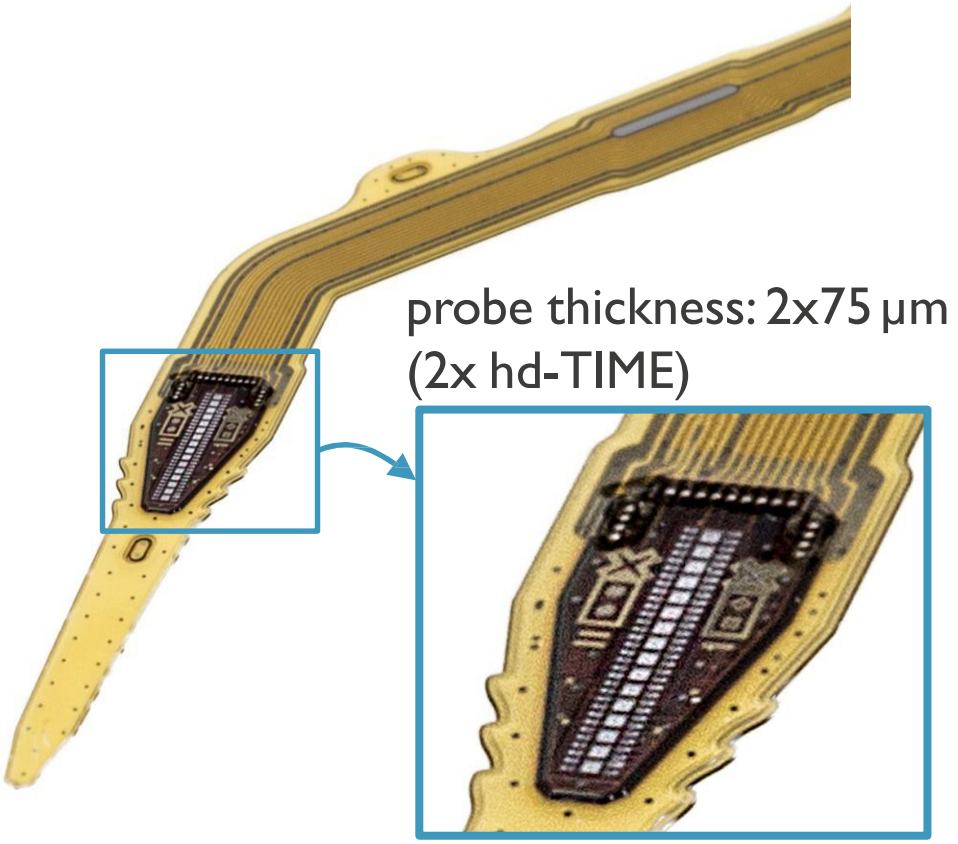
- **hd-TIME**:
  high-**d**ensity
  Transverse
  Intrafascicular
  Micro**E**lectrode



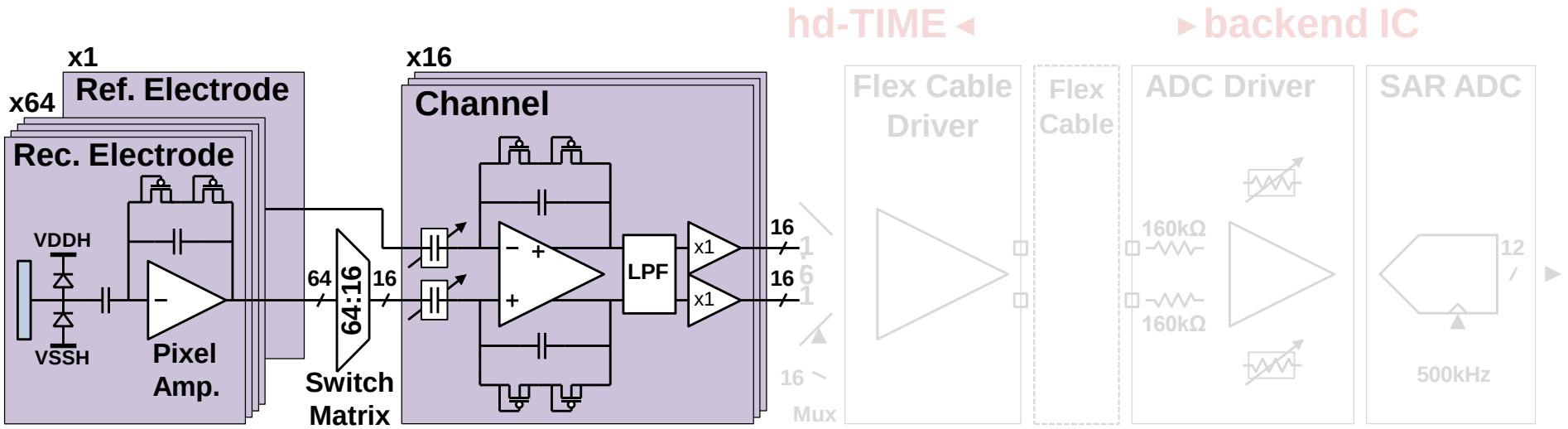
- Active probe: CMOS device + integrated electrodes implanted inside the nerve
  - bidirectional interface ← recording and stimulation
  - high electrode count with few external connections ← multiplexing
  - higher fiber selectivity ← transversal intra-fascicular implantation
  - higher signal ← local amplification
  - low power consumption ← power-efficient circuit design
  - minimum invasiveness ← chip thinning
  - long-term biocompatibility & stability ← custom chip encapsulation

Packaging

- IrO_2 electrodes deposition
- Laser cutting of embedding
- Back-to-back gluing



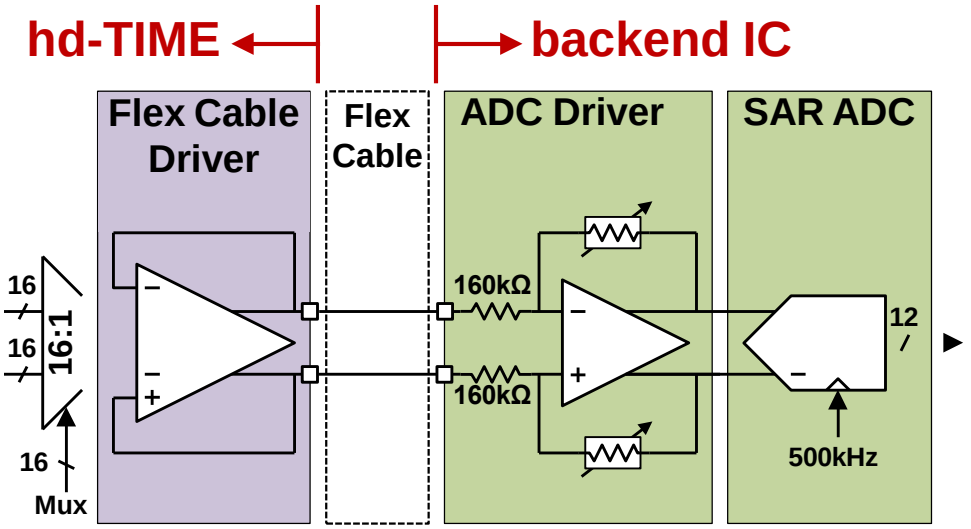
ENG Acquisition Chain



- 64 active electrodes
  - AC-coupled in-pixel amplifier: 24 dB, ~1 Hz HPF corner
- Switch-matrix
  - select best recording electrodes without need of repositioning the probe
- 16 channels for simultaneous readout
  - Programmable Gain: 4—44 dB

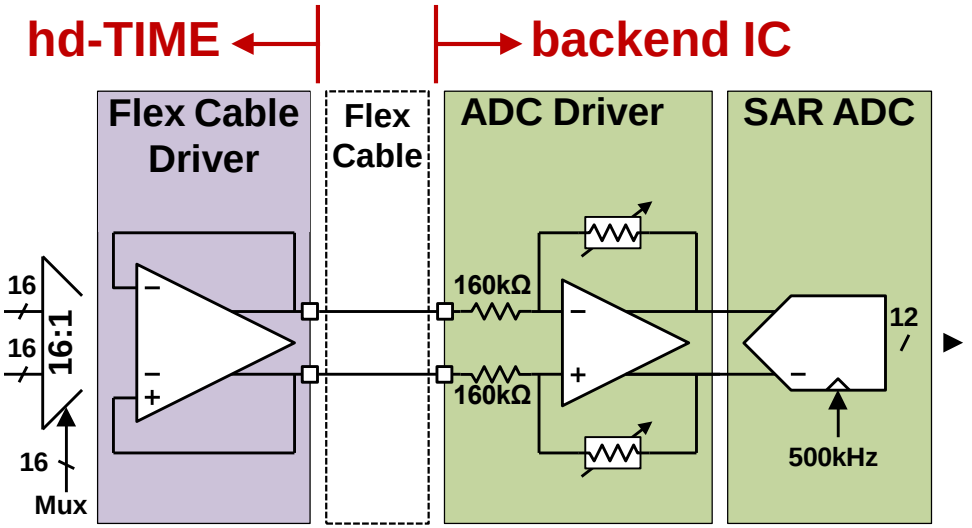
ENG Acquisition Chain

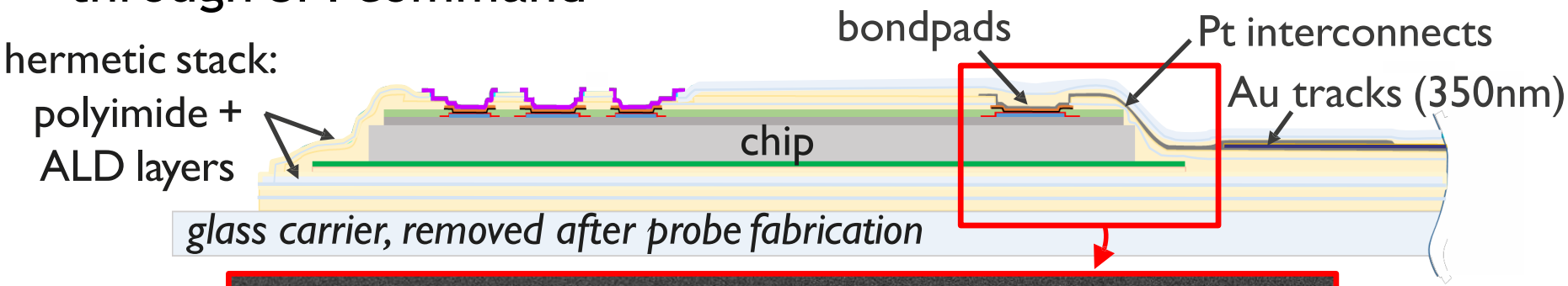
- Muxed at 31.25kHz/ch.
- Output driver
- ADC driver with programmable gain
- 12-bit 500kS/s SAR ADC
- synchronization MUX/ADC through SPI command

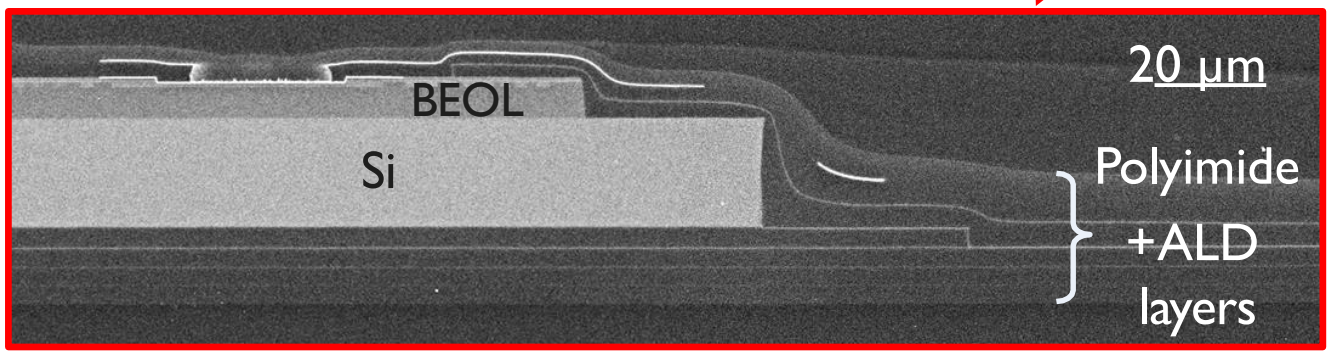


ENG Acquisition Chain

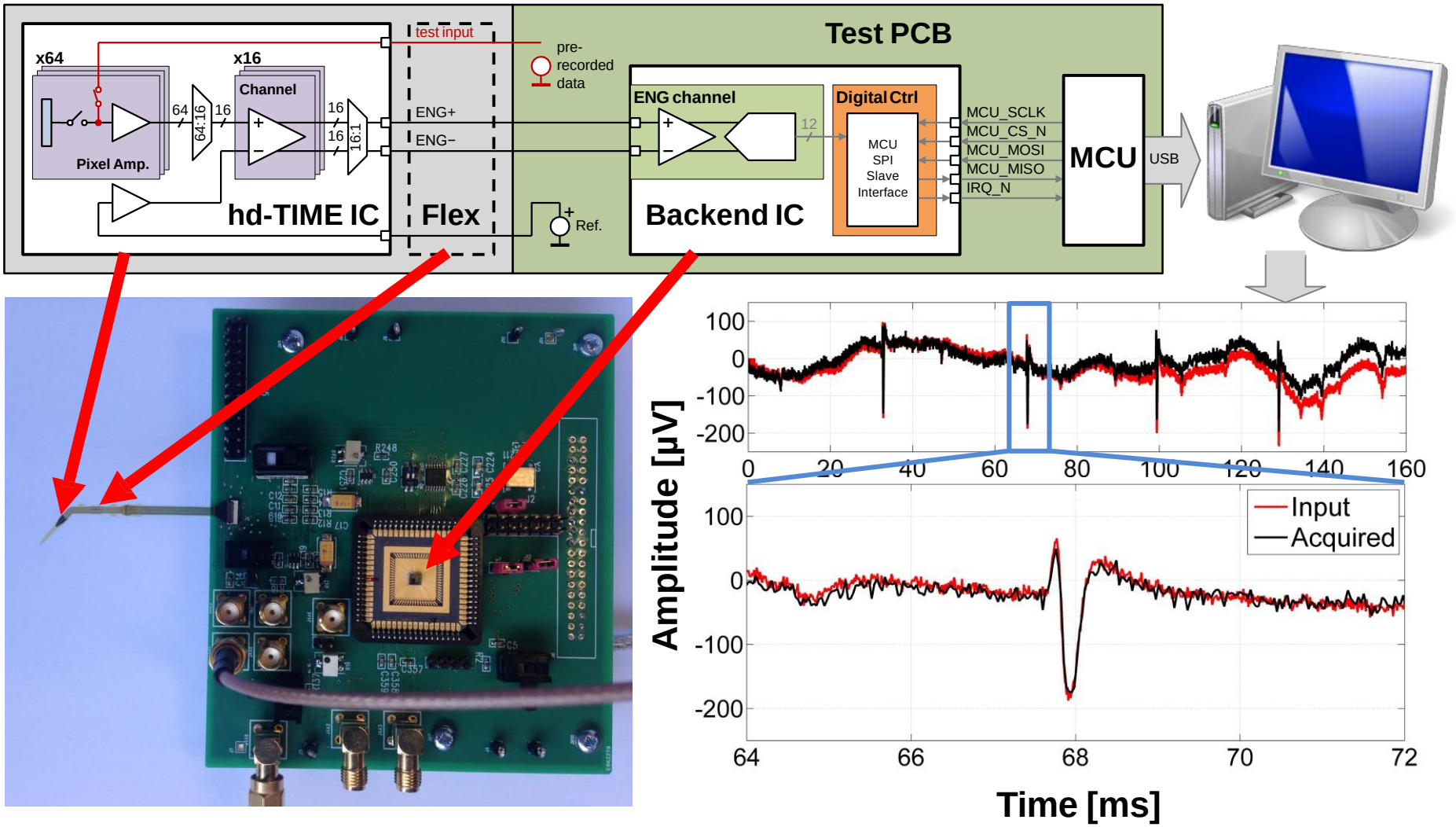
- Muxed at 31.25kHz/ch.
- Output driver
- ADC driver with programmable gain
- 12-bit 500kS/s SAR ADC
- synchronization MUX/ADC through SPI command







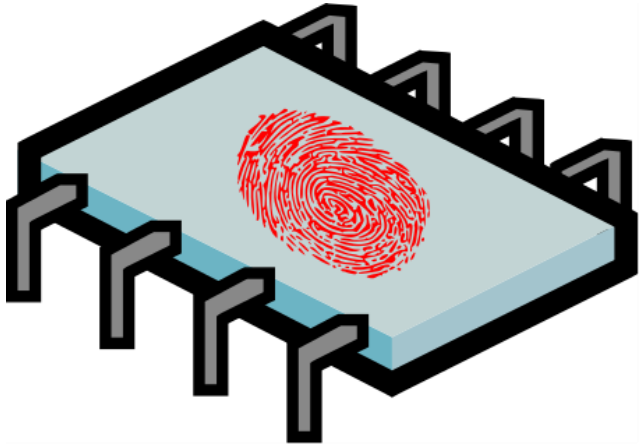
Measurement Results



- Acquisition of pre-recorded spikes through whole system

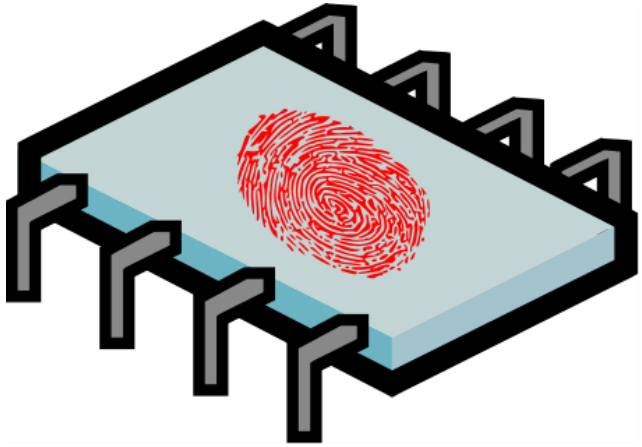
Physical Unclonable Function

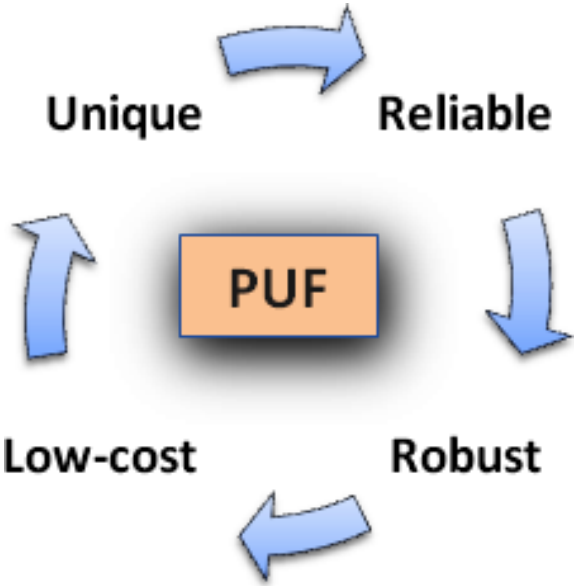
- **Used in**
  - **Cryptography**
  - **Chip identification**
  - **Obfuscation**
  - **…**



Physical Unclonable Function

- **Used in**
  - **Cryptography**
  - **Chip identification**
  - **Obfuscation**
  - **…**



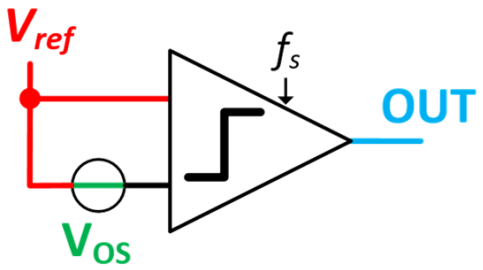


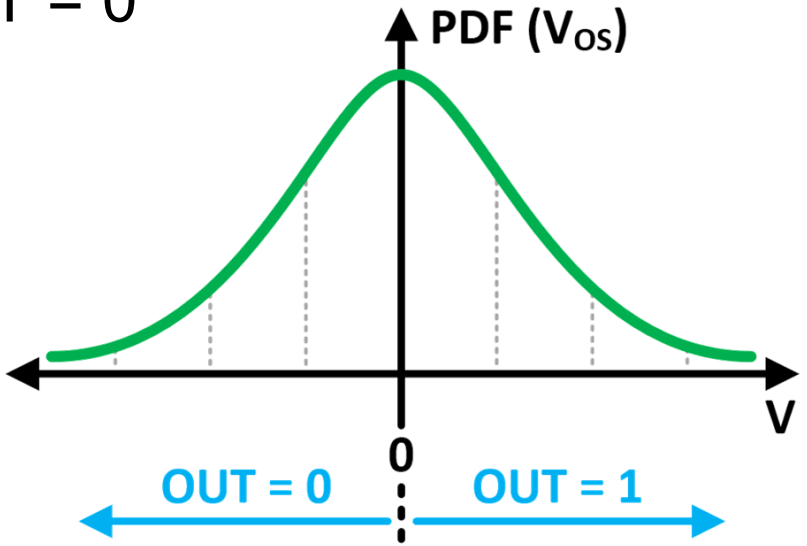
Our Approach

- **Create PUF for use in Analog/Mixed-Signal (AMS) applications**
  - Leverages process variations
- **Stochastic ADC based PUF:**
  - Easy identification in AMS chips
  - Can also be utilized in fully digital chips using standard cells
  - Simple design
  - Minimal hardware overhead with reuse of components readily available in most AMS chips

PUF Bit Generation

- Inherent random input offset voltage (V_{os}) of each comparator is normally distributed
- Employ V_{os} to generate a single bit (OUT)
  - Positive V_{os} → OUT = 1
  - Negative V_{os} → OUT = 0

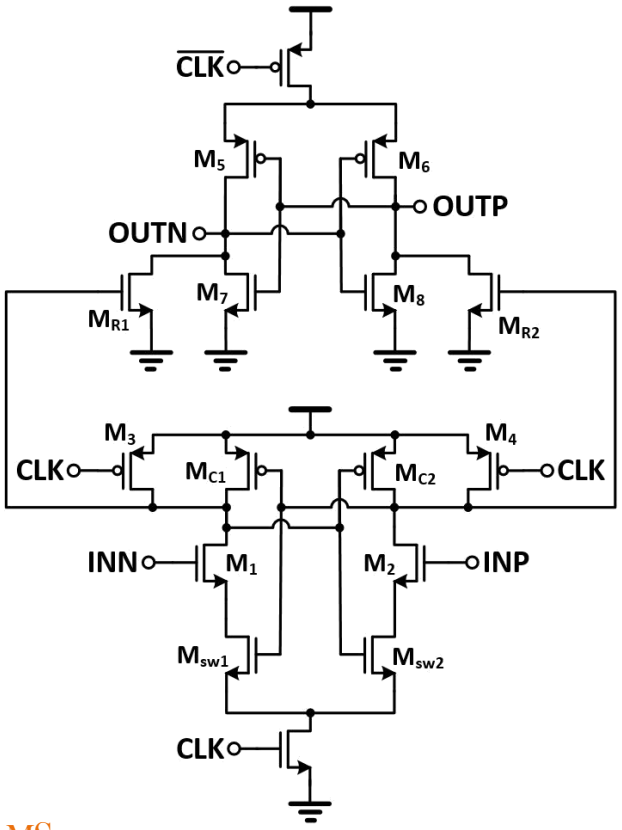




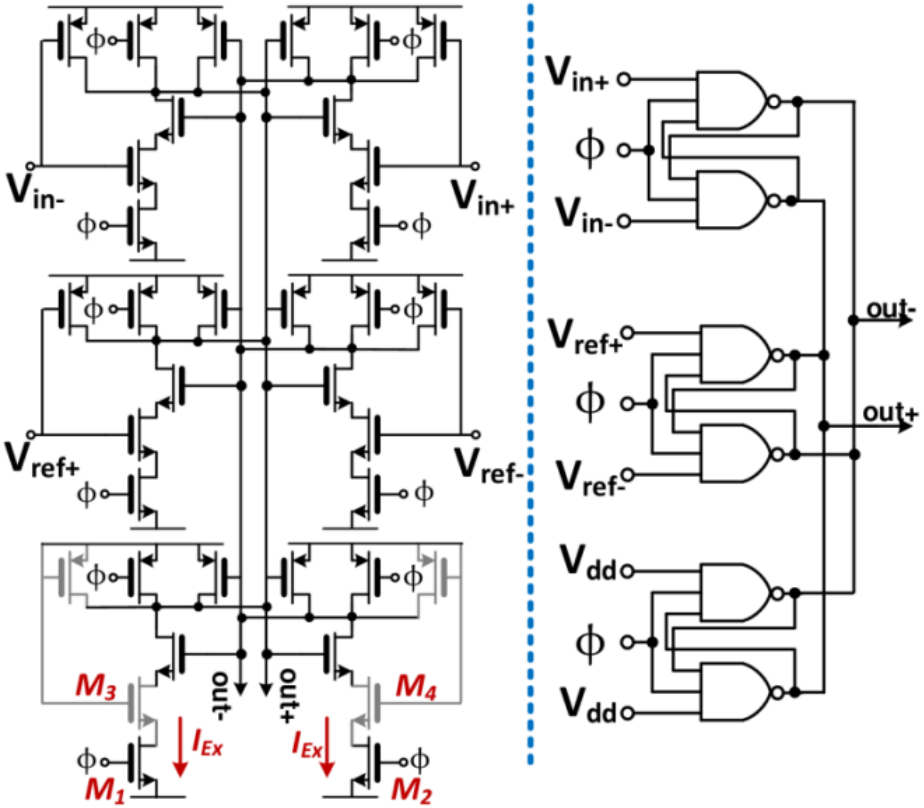
Proposed All-Digital Comparator

- **Compared with Custom Design**

Traditional Custom Designed Comparator (2-Tail)

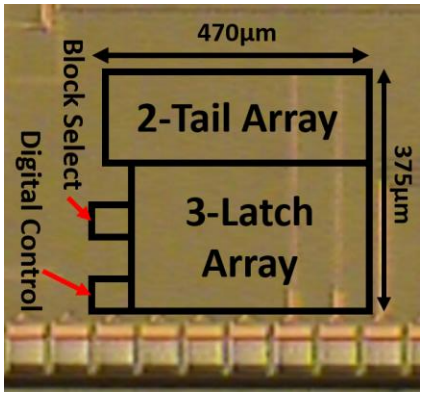


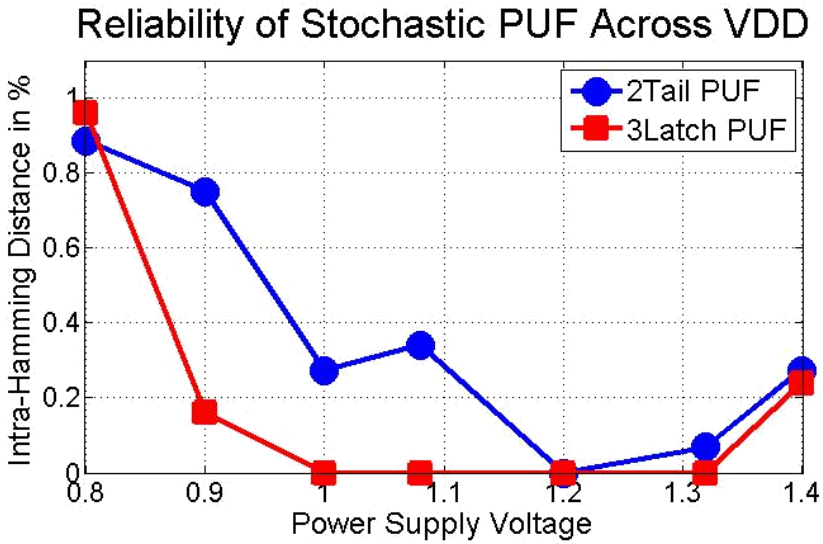
Proposed All-Digital Extended Offset Comparator (3-Tail)

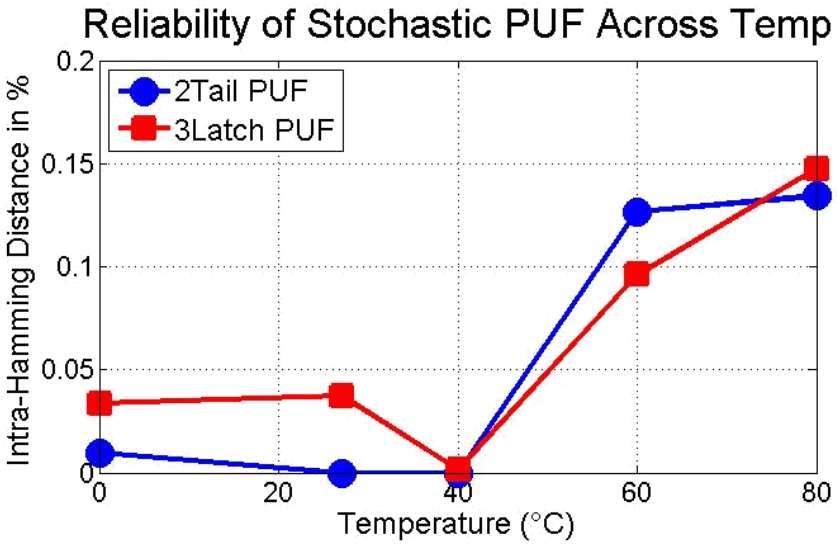


Measurement Results

- **Fabricated prototype***
  - Fabricated in 0.13µm CMOS process
  - Active area 0.144mm^2
- **Normalized Intra-HD**
  - Across VDD (0.8V – 1.4V)
    - 2-Tail: < 0.89%
    - 3-Latch: < 0.96%
  - Across Temp (0°C – 80°C)
    - 2-Tail: < 0.14%
    - 3-Latch: < 0.15%







Sponsored by National Science Foundation (NSF)

**IEEE International Symposium on Hardware Oriented Security and Trust (HOST) 2017*

Conclusions

- **Analog signals are everywhere**
  - **Even digital data requires analog signal processing techniques**
- **Different applications demand different specs**
  - **Audio → Very high linearity and resolution**
  - **Video → Medium BW and medium resolution**
  - **HD Video→ Medium BW and high resolution**
  - **BCI→ Very low BW and medium resolution**
  - **Communication →Large BW and medium resolution**
  - **…**

Conclusions

- **Analog signals are everywhere**

Every new application opens up new opportunities and brings new challenges in Analog/Mixed-Signal Domain

My Research & Sponsors

- **Scalable ADCs**
  - **Sponsored by SRC & Qualcomm Inc.**
- **Power Management**
  - **Texas Instruments, Analog Devices**
- **Analog Mixed-Signal Security**
  - **NSF, Honeywell**
- **Implantable Electronics**
  - **DARPA**
- **Sensor Interface**
  - **NSF**